Challenges of contact module integration for GaN-based devices in a Si-CMOS environment

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(Received 7 March 2014; accepted 22 April 2014; published 23 May 2014)

The authors report on the integration of an Au-free contact module intended for AlGaN/GaN high-electron-mobility transistors fabricated in a 200 mm Si complementary metal–oxide–semiconductor facility. Contacts are characterized via transfer line method structures, tunneling electron microscopy, and energy-dispersive x-ray spectroscopy. Factors leading to incorrect extraction of contact resistance are discussed. The authors find that reoptimization of chemical vapor deposited silicon nitride on AlGaN/GaN substrates is required to ensure reliable determination of contact resistance, gate-to-source spacing, and gate-to-drain spacing. Additional process development is required to enable parallel processing of Si and GaN devices. © *2014 American Vacuum Society*.
[http://dx.doi.org/10.1116/1.4874801]

I. INTRODUCTION

III-nitride semiconductors have many useful material properties such as wide bandgap, high thermal conductivity, and high critical breakdown field. Additionally, spontaneous and piezoelectric polarizations allow the formation of two-dimensional electron gases at III-N interfaces with high density and high electron mobility. Applications involving operation at high speed and power require the switching transistors to withstand high electric fields in the "off" state and to have minimum conduction loss in the "on" state. The unique combination of high electron mobility and high breakdown strength of the III-nitride family make them attractive to such applications.[1]

To compete with Si in terms of cost, it is important to enable high-volume production and compatibility with existing Si-CMOS infrastructure. Au-free technology is required to meet the strict contamination rules of a CMOS processing line and has been recently demonstrated on AlGaN/GaN high electron mobility transistors (HEMTs).[1–4] Moreover, AlGaN/GaN epitaxy has gone through intense optimization,[5] and its high quality growth (with a low wafer bow) on 200 mm Si wafers has been made possible by the use of thick Si substrates and stress mitigating layers.[6] Combining Au-free technology with the use of 200 mm substrates can drive down manufacturing costs significantly and allow parallel processing of CMOS and GaN product as well as facilitate cointegration of Si and GaN-based devices. Integration of Au-free AlGaN/GaN technologies in 200 mm CMOS fabrication environments is beginning, with initial focus on manufacturable methods to realize enhancement mode operation, ways to avoid/mitigate Ga tool contamination, and Au-free ohmic contacts.[6,7] Two primary metallizations are being explored for ohmic contact: Ti-based[1–3] and Ta-based.[7,8] While Au-free ohmic behavior has been realized with both these material systems, optimization of contact resistance and uniformity is challenging. Additionally, wafer/ tool interaction is more complex with GaN-based wafers compared to silicon. For instance, extreme wafer warp can cause robot breakage and depth of focus issues in lithography, while pocket carrier wafers can drastically change materials parameters during plasma processing. Finally, ohmic contact formation often requires a high temperature anneal (>800 °C),[1] which inhibits the use of gate-first process flows. In light of the need for continuing development, this Letter discusses some of the challenges and solutions associated with the integration of ohmic contacts to AlGaN/GaN in a Si-CMOS environment.

II. EXPERIMENTAL DETAILS

Sample fabrication took place in a 200 mm CMOS fab using an Au-free process. GaN (2 nm)/$Al_{0.24}Ga_{0.76}N$ (17.5 nm)/GaN on Si (4 in. diameter) obtained from Nitronex Corporation[9] were used as substrates with a total buffer thickness (including transition layers) of 2 μm. The processing was performed on 200 mm Si pocket wafers containing both AlGaN/GaN-on-Si wafers and Si control wafers. All wafers progressed through the line in parallel with Si CMOS lots. Tool contamination was monitored using total reflection x-ray fluorescence, and typical results are reported elsewhere.[7] The epiwafers were cleaned in HCl:H_2O (1:10) for 10 min and passivated with 900 Å Si_xN_y using plasma

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enhanced chemical vapor deposition (PECVD) at 410 °C. The silicon nitride layer is used to passivate the AlGaN surface states by acting as an effective moisture barrier.[10,11] Nitride is typically preferred over oxide to mitigate oxygen doping of the III-N semiconductors.

Isolation was provided between the different devices via multistage N^+ ion implantation with photoresist serving as the mask. Contact windows of dimensions 21.5 × 94 μm^2 were opened in the Si_xN_y using CF_4 based reactive ion etching. A subsequent AlGaN barrier recess etch is believed to improve both contact resistance[1] and its uniformity across a wafer;[2] however, for the sake of simplicity, no recess was employed in our work. A HCl:H_2O (1:10) premetallization clean was performed immediately prior to the deposition of the Ta/Al/Ta (7/200/20 nm) metal stack with DC sputtering. The metal was patterned using a Cl_2/BCl_3 based plasma etch and followed by a rapid thermal anneal at 575 °C for 4 min in N_2 ambient to enable ohmic contact formation. Figure 1 shows the final device structure and transfer line method (TLM) spacing (d), which was varied across the sample.

Four probe IV measurements were acquired with a Hewlett-Packard 4145 parameter analyzer in the dark at room temperature to calculate the resistance of the TLM structures. The resistance normalized by unit width (ohm-millimeter) was plotted against TLM spacing (as confirmed by top down SEM). Contact resistance was extracted by extrapolating the linear curve to the $d = 0$ axis and dividing the result by two.[12]

Scanning tunneling electron microscopy (STEM) was used to study the ohmic contact in the neighborhood of the contact window edge. Samples for STEM were prepared by single beam focused ion beam. Also, bulk samples (AlGaN/GaN and Si control samples) with Si_xN_y passivation layer were prepared for x-ray reflectivity (XRR) characterization.

III. DISCUSSION

Figure 2 shows the resistance versus TLM spacing plot for the devices fabricated as described in the experimental section. Reference TLM data without nitride passivation on a similar nitride heterostructure is included where no superfluous effects are observed. Although ohmic behavior is observed, the extracted contact resistance is negative, indicating an error in spacing estimation or a secondary, parallel conduction path. The rest of this Letter focuses on determining the reason for obtaining negative or extremely low contact resistance.

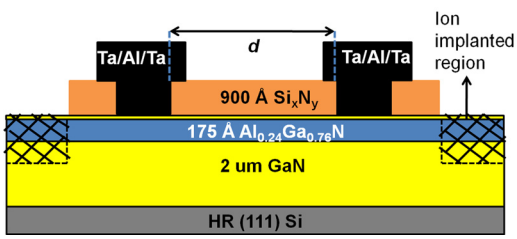

FIG. 1. (Color online) Cross-section schematic of the final TLM structure with TLM spacing d (transition layer details are not shown).

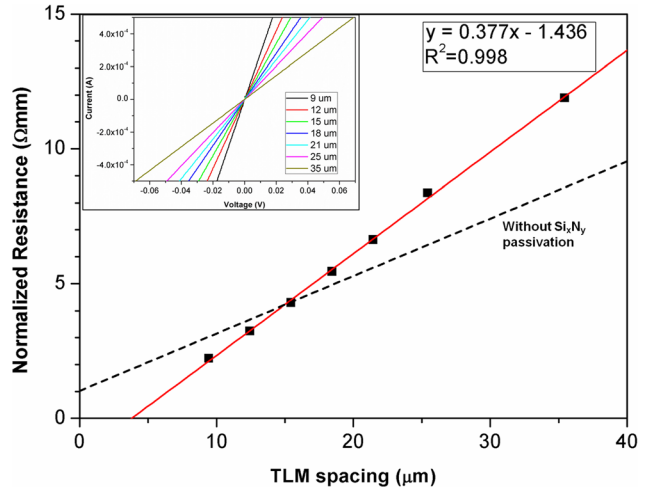

FIG. 2. (Color online) Plot of normalized resistance vs TLM spacing for ohmic contact structures integrated with and without Si_xN_y passivation. The y-intercept (which gives twice the contact resistance) is negative. Inset: I-V data for sample with passivation.

Figure 3 shows a STEM image and the EDX line scan acquired along the line shown near the contact window edge after the postmetallization anneal. Aluminum has diffused into the Si_xN_y passivation layer forming a uniform layer of aluminum-diffused silicon nitride (abbreviated as Al-Si-N henceforth). The Al is believed to originate from the Ta-Al ohmic metal alloy, not from the AlGaN. SIMS profiles collected before and after anneal (not shown) indicated little change in the Al concentration of the AlGaN. Since there is

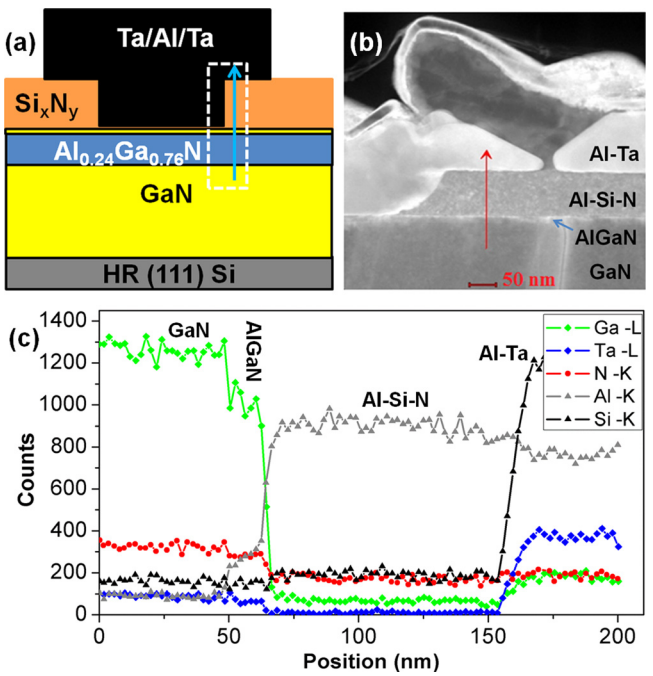

FIG. 3. (Color online) (a) Cross section schematic showing the position (contact window edge) of the STEM image and the EDX linescan. (b) STEM image at the contact window edge. Agglomeration and formation of multiple Ta-Al phases due to the alloying anneal are visible. (c) EDX linescan along the line marked in (b). Aluminum has diffused into the Si_xN_y layer uniformly forming Al-Si-N.

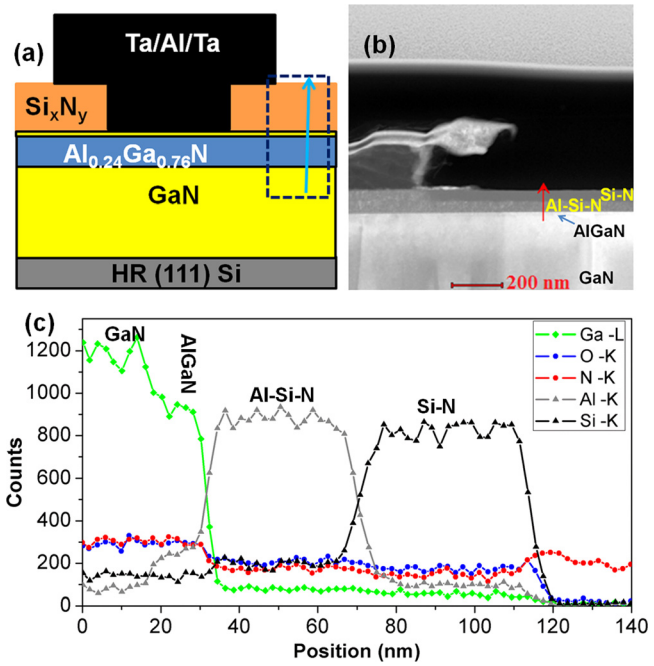

FIG. 4. (Color online) (a) Cross section schematic showing the position (outside the metal overlay) of the STEM image and the EDX linescan. (b) STEM image outside the contact metal overlay (c) EDX linescan along the line marked in (b). Instead of a single Si_xN_y layer, there is also an Al diffused SiN (Al-Si-N) layer in contact with the AlGaN/GaN heterostructure.

overlap between the Ta-M and Si-K lines, we report the Ta-L signal to aid in the decoupling of Si and Ta composition. Hence, an increase in the Si-K signal without a simultaneous increase in the Ta-L signal is attributed to a true increase in silicon composition. Similarly, a Ta Auger line interferes with the Ga-L line, leading to an increase of the Ga signal in Ta-rich regions [far right of Fig. 3(c)]. The nitrogen signal observed throughout the EDX linescan is physical and arises from multiple sources. Ta is expected to getter nitrogen from the III-N during alloy anneal due to the low enthalpy of formation of TaN, and, given that the primary point of this paper is the importance of the quality of the SiN film, nitrogen may have out-diffused out from the SiN.

Figure 4 shows another STEM image and corresponding EDX linescan captured outside the contact metal edge. Again, Al has diffused into the Si_xN_y layer forming Al-Si-N, in this case, preferentially along the Si_xN_y/AlGaN interface. Hence, from the STEM image and EDX scans it is clear that there is significant Al diffusion into the Si_xN_y passivation layer, more than 0.5 μm beyond the metal overlay (3 μm).

Diffusion of Al has been previously reported in Si_xN_y containing oxygen impurities and has been extensively studied by Ogata *et al.*[13] The in-depth aluminum diffusion profiles observed by Ogata *et al.* reveal that Al diffuses completely through a 50 nm thick Si_xN_y film after a 60 min anneal at 530 °C. Oxygen impurities are common in PECVD films and likely contribute to the Al diffusion; however, in our study, the STEM image of Fig. 4(b) indicates that aluminum has diffused more than 0.5 μm after just a 4 min anneal at 575 °C. Hence, the rate of aluminum diffusion is significantly accelerated (greater than 50 times) as compared to the reference.[13] This suggests an additional mechanism driving the formation of Al-Si-N.

Formation of Al-Si-N will affect the extraction of contact resistance through TLM in the following manner. The conducting channel length (effective TLM spacing) is no longer defined by lithography. The diffusion of Al enables contact beyond the contact window, which reduces the channel length. Here we see as much as a 7 μm reduction. Hence, instead of using the designed TLM spacing, a reduced spacing must be used in the contact resistance extraction. This spacing is difficult to accurately determine as the conductivity of the Al-Si-N layer is unknown and presumably varies with the Al content.

Obtaining a negative value for contact resistance is sufficient for suspecting Al-Si-N formation, but it is not a necessary condition. Since, the TLM spacing reduction depends on the amount of diffusion of Al into the Si_xN_y film, it is also possible to obtain seemingly low values for contact resistance (non-negative). It should be noted here that the nonuniformity of extracted contact resistance across the wafer is yet another indication of the poor quality of the deposited Si_xN_y. Figure 5 shows R versus d plot from a different region of the wafer. The extracted contact resistance is 0.01 Ω·mm which can be incorrectly interpreted as an extremely good ohmic contact. Moreover, further process steps to the device structure in Fig. 1 could include the formation of a gate for use as a HEMT. If Al diffusion into Si_xN_y goes unnoticed, breakdown voltage will degrade due to reduced gate-to--source and gate-to-drain lengths. In the case of extreme lateral scaling, the device may even be shorted. Hence, from a process development standpoint, it is crucial to ensure that Al-Si-N is not formed during process integration.

XRR performed on as-deposited silicon nitride on an AlGaN/GaN substrate revealed that the density of the Si_xN_y layer was around 4.4 g·cm^{-3}, indicating a highly Si rich

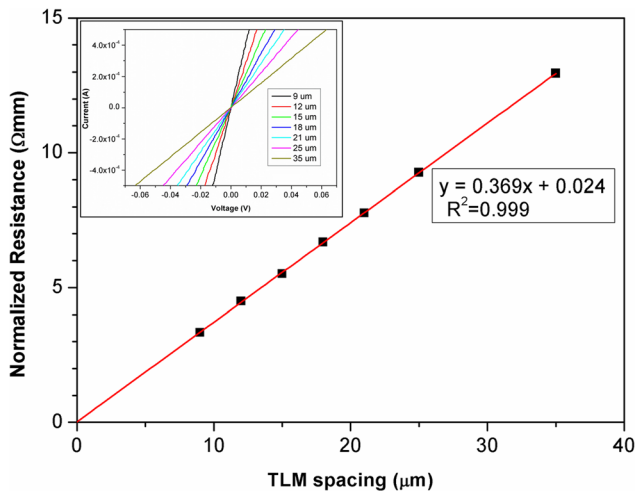

FIG. 5. (Color online) TLM plot from an alternate region of the substrate. The contact resistance can be incorrectly interpreted as being extremely low due to Al diffusion. Inset: I-V data for corresponding test structures.

layer.[14] Also, the calculated N/Si ratio from the EDX linescan [Fig. 4(c)] is around 0.5, congruent with the conclusion made from XRR. Hence, we infer that a Si-rich Si_xN_y passivation layer leads to accelerated diffusion of Al, resulting in inaccurate extraction of contact resistance. It was also observed that the Si_xN_y density on a Si control sample (also processed in a pocket wafer) was approximately 2.5 $g \cdot cm^{-3}$. This value is similar to the qualified value for the standard 200 mm CMOS process, indicating that the change in thermal conduction due to the pocket wafer is not the primary cause of the density change. Moreover, postdeposition anneal of Si_xN_y in nitrogen ambient, prior to the ohmic contact module, did not inhibit Al diffusion. Hence, Si_xN_y PECVD (and likely all CVD processes) must be optimized on AlGaN/GaN directly, separate from the standard Si process, to achieve a proper index of refraction and density.

IV. CONCLUSIONS

The challenges associated with the parallel integration of ohmic contacts to AlGaN/GaN in a 200 mm Si CMOS environment were studied. STEM images and EDX scans revealed significant Al diffusion into the silicon nitride passivation layer after ohmic contact processing. Consequently, this can lead to inaccurate extraction of contact resistance, degradation of breakdown voltage and, possibly, shorting of the device. XRR measurements lead to the conclusion that Si-rich Si_xN_y was the reason behind accelerated Al diffusion. The optimization of PECVD Si_xN_y on AlGaN/GaN, qualified independently from the standard Si process, is necessary to achieve a proper index of refraction and density for Si_xN_y, which in turn will lead to smooth integration of ohmic contacts to AlGaN/GaN in a Si CMOS environment. Additional research is required to develop a stoichiometric process for cointegration of both Si and GaN devices.

ACKNOWLEDGMENTS

Special thanks to John Roberts of Nitronex Corporation for providing critical understanding of the AlGaN/GaN on Si substrates. This work was supported in part by the Texas A&M University National Excellence Fellowship, National Science Foundation Grant ECCS-1028910, and the Office of Naval Research Grant N00014-12-1-0971.

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