PATTERNING TRI-HALIDE PEROVSKITE SINGLE CRYSTAL GROWTH

by

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A thesis submitted to the Graduate Council of
Texas State University in partial fulfillment
of the requirements for the degree of
Master of Science
with a Major in Physics
December 2021

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DEDICATION

This work is dedicated to Dr. Alexander Zakhidov, who passed away before the completion of this thesis project. As well as to everyone in the physics department who helped and supported this research, including Dr. Yoichi Miyahara, Dr. Wilhelmus Geerts, and Dr. Casey Smith for their advice, guidance, and help in the labs. Lastly, it is dedicated to my family who have always supported me.

ACKNOWLEDGEMENTS

This research was in part supported by the U.S. Department of the Navy via a HBCU/MI grant (ONR grant no. N000141912576), by the National Science Foundation (EPMD grant #1906492 and STTR Phase II grant #1927020) and by a grant from DOE (DE-EE0009526).

Part of this work was presented at the XXIX International Materials Research Congress meeting (MRS): Drew Amyx, Alex Zakhidov, Craig Swartz, “Patterned Single Crystal Perovskite Field-Effect Transistors”, XXIX International Materials Research Congress meeting (MRS), August 15-20, 2021.

I would like to thank Dr. Alexander Zakhidov for his invaluable support, and knowledge of perovskite research & physics in general, he will always be missed. I would also like to thank Dr. Yoichi Miyahara for agreeing to be my advisor on such short notice, and Dr. Wilhelmus Geerts for leading the grants held by Dr. Alexander Zakhidov, and Dr. Casey Smith for his continued help in the lab, advice on process improvements such as photolithography, and for the trainings given by him on equipment in both the ARSC and NRSC. Additionally, I want to thank my peers in research, Nischal Khakurel, Leobardo Rodriguez, and Patrick Kollias for their help and useful discussions when making substates and samples. Lastly, I want to thank the people in Dr. Miyahara’s research group for their research support and presentation advice; Noah Austin-Bingamon, Mitchell Ford, Tan Nguyen, Binod D. C., Sunil Adhikari, John, Dickenson, Cameron Gonzalez, Dr. Dip Mahato, Rigo Mayorga-Luna, Gabriel Mestas, Iris Okoro, Johnathin Sims, Ethan Rivers, Shashank Neupane, and Anthony You.

TABLE OF CONTENTS

Page

LIST OF TABLES

Table **Page**

LIST OF FIGURES

Figure **Page**

LIST OF ABBREVIATIONS

Abbreviation	Description
PCE	Power Conversion Efficiency
NREL	National Renewable Energy Laboratory
CVD	Chemical Vapor Deposition
ITO	Indium Tin Oxide
PTAA	poly(bis(4-phenyl)-2,4,6-trimethylphenylamine
FET	Field Effect Transistor
BC	Bottom Contact
TC	Top Contact
RF	Radio Frequency
NRSC	Nanofabrication Research Service Center
PR	Photoresist
UV	Ultraviolet
TMAH	Tetramethylammonium Hydroxide
DI	Deionized
ICP	Inductively Coupled Plasma
RIE	Reactive Ion Etching
SD	Source-Drain
$MAPBr_3$	Methyl-Ammonium Lead Tri-Bromide
MABr	Methyl-Ammonium Bromine

DMF	N,N-Dimethylformamide
XRD	X-ray Diffraction
SEM	Scanning Electron Microscopy
EDS	Energy Dispersive Spectroscopy
AFM	Atomic Force Microscope
FWHM	Full Width at Half Max
RMS	Root Mean Square
PDMS	Polydimethylsiloxane

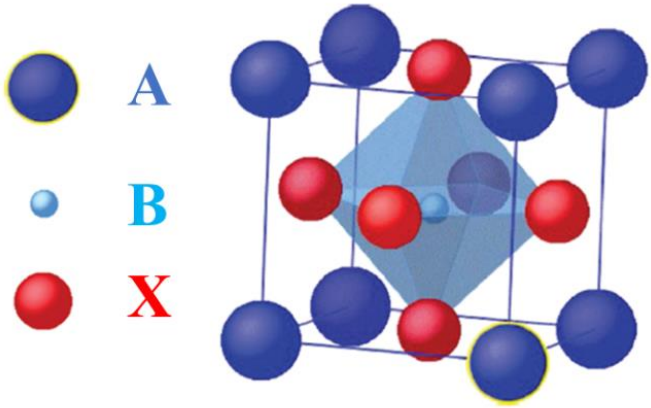
ABSTRACT

Organic perovskites have been growing in the field of organic electronics, and lately field-effect transistors with single-crystalline perovskites have received more attention, because they should have ideal field-effect mobility and new crystal growth techniques have made them easier to synthesize. This research works to improve the reproducibility of the single-crystal growth as well as pattern the perovskite single crystals for better device reproducibility. We were successful in patterning the crystal growth, using silicon chips patterned via photolithography, and a custom-made clamp to even the pressure applied to the substrates. However, improved contact between the substrates and better control over the pressure applied during the annealing process is needed to improve the quality of the patterned crystal growth.

I. INTRODUCTION

History of Perovskites

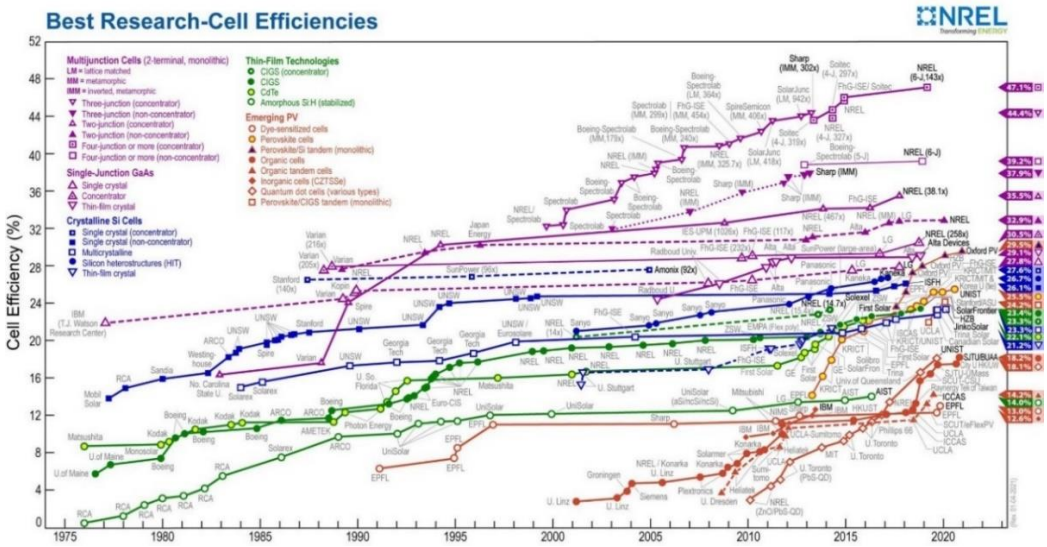
In 1839 Gustav Rose, a Russian mineralogist discovered the perovskite structure in the Ural Mountains. However, it was not until 2009 when Tsutomu Miyasaka et al. used perovskite materials on a TiO_2 layer to make a solar cell with a power conversion efficiency (PCE) of 3.8% that was stable for a few minutes[1]. The perovskite structure, shown in Figure 1[2], is electrically neutral and follows a general ABX_3 formula, A and B being cations and X being an anion. The stability of the structure is determined using the Goldschmidt relationship, $t_{IR} = (R_a + R_x)/\sqrt{2}\,(R_B + R_x)$, here R_A, R_B, and R_X are the ionic radii of the ABX ions. Perovskites generally form when $0.9 < t_{IR} < 1.1$, outside of this range causes more impurities to form, preventing crystal formation[2].



[Figure 1: Basic cubic perovskite cell.]

The National Renewable Energy Laboratory (NREL) publishes a chart tracking the progress of solar cell PCE on a yearly basis. In Figure 2 below you can see the growth in perovskite solar cell efficiency has been significant, starting at about 14% PCE in 2013, and ending with 25.5% PCE in 2021[3]. Perovskites also have a direct band gap which can be tuned via halide mixing increasing the interest in the material for a variety

of uses[4]. Particularly solar cells because the direct band gap determines the spectral range of photon absorption for hole pair generation used to drive an electrical load or charge a battery. This increase in interest is bolstered by the simple processability and low price of materials required to make devices compared to silicon-based electronics. For example, slot-die coating is a wet deposition technique that can be scaled up for manufacturing, where a die head deposits perovskite solution as it moves over substrates, or as the substrates move under it, resulting in an even polycrystalline coat over the surface. This deposition process can even be done in air instead of an inert atmosphere such as nitrogen[5]. However, the solvents used to dissolve the perovskite materials like DMF and DMSO are harmful, so protection such as a fume hood or glovebox is still required.



[Figure 2: NREL solar cell efficiencies.]

Most devices are made with polycrystalline perovskite material because that is the result from spin-casting the precursor solution. However, these devices tend to have lower field effect mobility due to grain boundaries between crystals. Advances have been made in the growth techniques of single crystals as well, and this research expands upon those techniques.

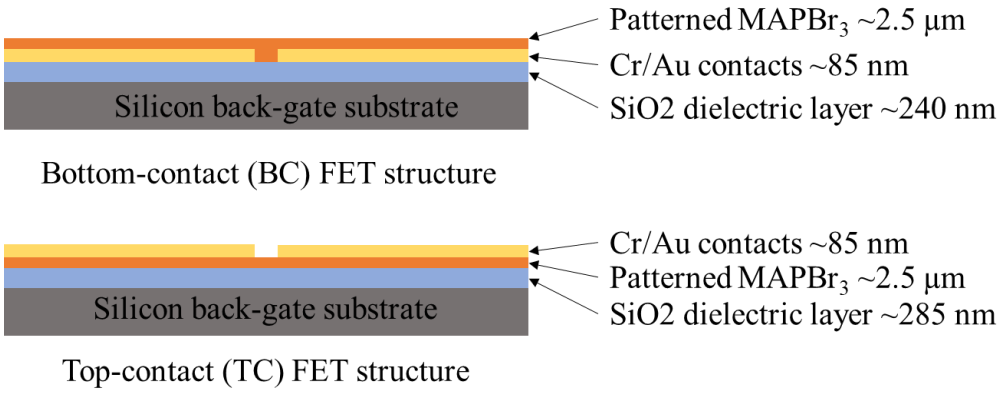
Single crystal perovskites have been grown using chemical vapor deposition (CVD)[6], solution-assisted growth[7], and space confined growth[8]. Through these techniques, people like Shen et al. can synthesize large single crystalline perovskites on the millimeter scale, allowing them to experimentally determine the lattice constant for $MAPBr_3$, 0.59062 nm[9]. However, the CVD and solution-assisted growth techniques both have a more complex process and require more materials to perform than the space confined growth technique developed by Weili Yu et al. This crystal growth technique only requires a clamp and two substrates, (for example ITO coated glass), as well as a perovskite precursor solution. However, there is a downside to this growth method, as the device creation is not easily reproducible because the single crystals grown cover a low surface area of the substrate rather than covering the entire substrate's surface.

Attempts to improve the reproducibility of the space-confined growth technique have been made by including a hydrophobic layer such as poly(bis(4-phenyl)-2,4,6-trimethylphenylamine (PTAA)[10]. This increases the surface contact angle of the perovskite solution, reducing the amount of possible nucleation sites so the crystals grow closer together, making them more likely to add to one crystal instead of forming multiple smaller ones. The increased hydrophobicity also allows the perovskite solution to be drawn into a sample with capillary action more easily[11]. Additionally, PTAA is commonly used in perovskite solar cells as a hole transport layer.

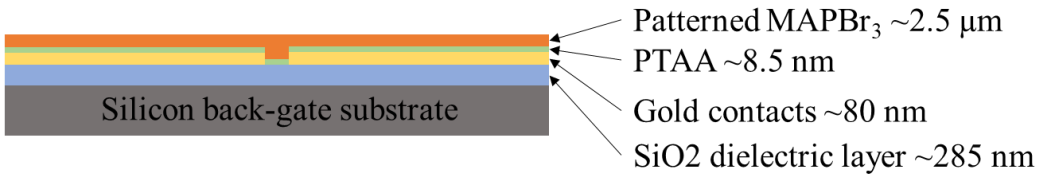
This Research

The goal of this research is to improve the single crystal growth and the device reproducibility of the space-confined growth method, by using a patterned silicon substrate to direct the precursor solution. We chose to use patterned silicon because it is a

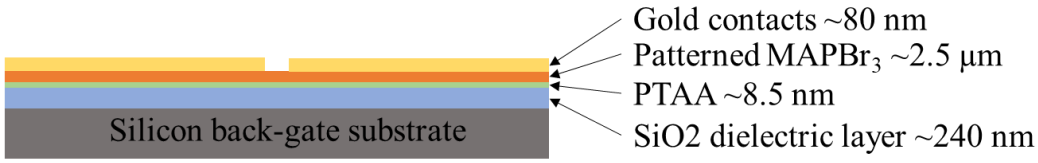
widely used material in device architecture and can be patterned to direct crystal growth. Additionally, there were thickness inconsistencies when using thin films to space our substrates such as polyethylene terephthalate (PET) or thin aluminum foil due to folding during the clamping of the two substrates. To compare our results to Weili Yu et al. we made two different types of field-effect transistor (FET) structures, bottom gate bottom contact (BC) and bottom gate top contact (TC), both of which use a silicon substrate as the gate, and SiO2 as the dielectric. The main difference is the position of their source-drain gold contacts, for BC transistors the gold contacts are deposited and patterned before crystal growth. In the case of TC transistors, the contacts are deposited through a shadow-mask after crystal growth; we use a shadow-mask to avoid washing away the crystals with the gold wet etch patterning process. The schematics for these transistor structures are shown below in Figure 3 and the inclusion of PTAA for increased substrate hydrophobicity and larger single crystal growth is in Figure 4.



[Figure 3: Bottom contact and top contact transistor structures without PTAA.]



PTAA coated bottom-contact (BC) FET structure



PTAA coated top-contact (TC) FET structure

[Figure 4: BC and TC transistor structures with PTAA.]

II. METHODOLOGY

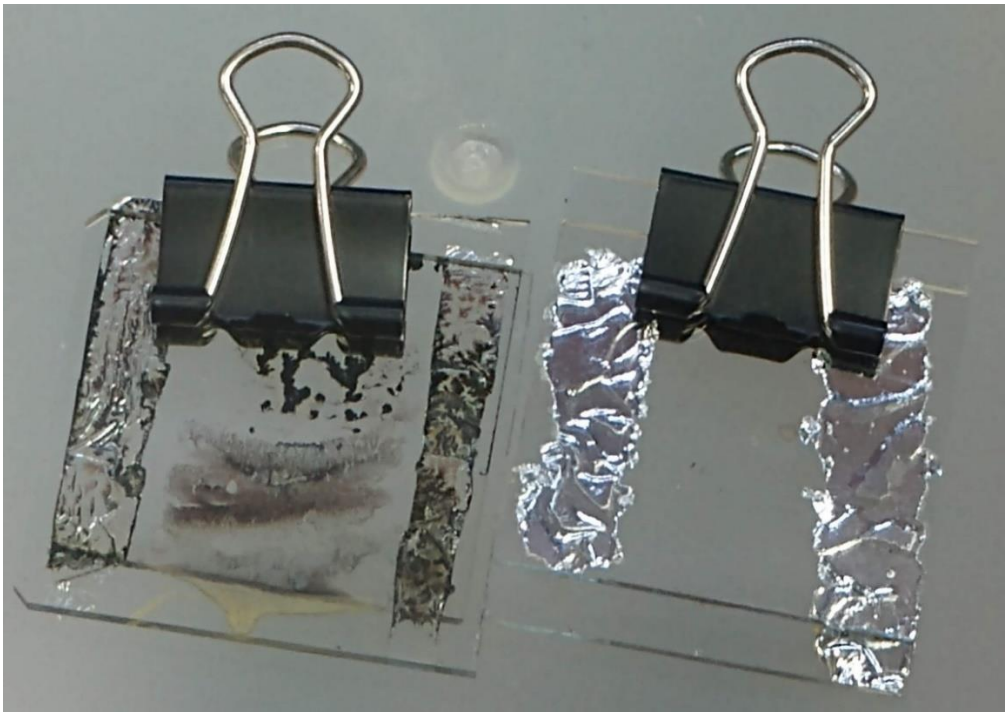
Initial Research

We first tried to replicate the results of Weili Yu et al.[8] by using glass slides that were separated by a 2.5 μm film to grow $MAPBr_3$ single crystals. The glass slides were sonicated for 30 minutes in a solution composed of 475 mL of distilled water and 25 mL of deconex op 121 glass cleaner. The glass substrates were then rinsed with distilled water and sonicated for 30 more minutes in 500 mL of distilled water. After sonication, the slides were blow dried with a dry nitrogen air gun and exposed to an oxygen based plasma for 10 minutes in a radio frequency (RF) plasma cleaner, Figure 5 shows the area where this process was carried out.

[Figure 5: Ultra-sonicator on far left and RF plasma cleaner on far right.]

Once the slides were clean, strips of 2.5 μm thick PET were cut and placed between the glass slides which were then clamped together with a binder clip and annealed at 270°C for 5 minutes to adhere the substrates together. Ideally the space between the glass slides after annealing is 2.5 μm, but we noticed wrinkling in the PET

film as the glass slides were clamped together which tended to increase the thickness of our samples. To avoid this, we tried using 2.5 μm thick aluminum foil strips in the hopes of it being more rigid, however it was prone to wrinkling as well, the two different samples are shown below in Figure 6. This wrinkling effect is what prompted us to pattern silicon substrates to control the thickness between the substrates more easily.



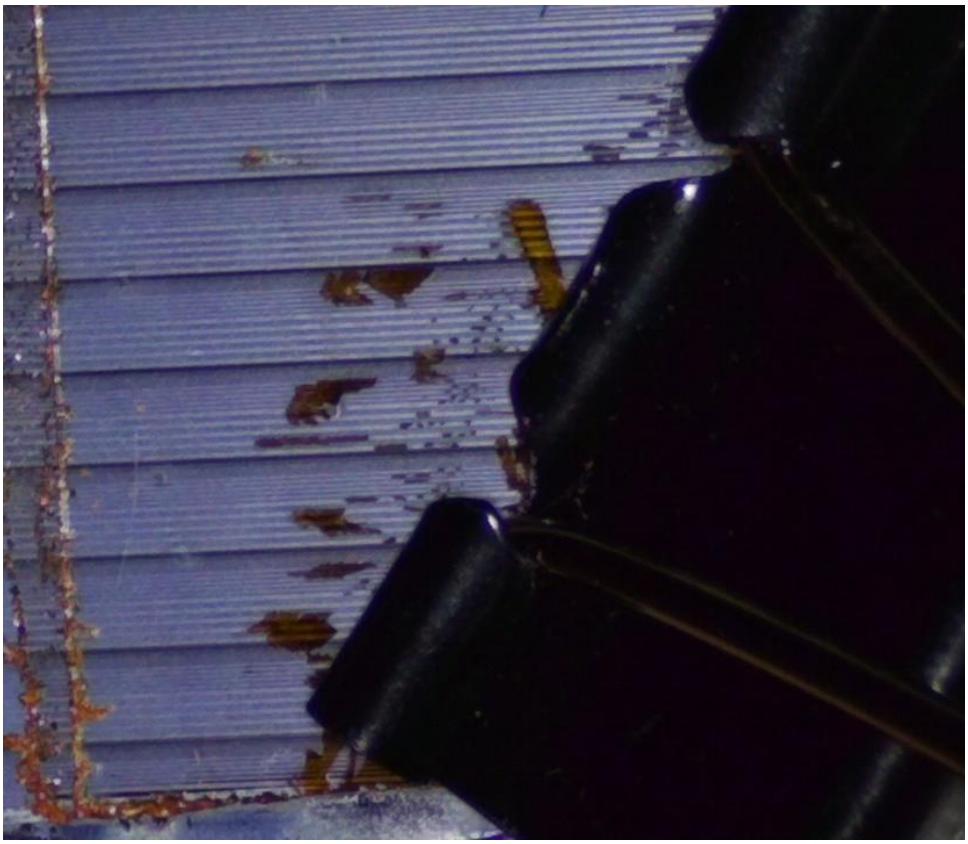
[Figure 6: Left is PET-spaced sample after crystal growth, right is Al-spaced sample before crystal growth.]

[Table 1: Annealing conditions for $MAPBr_3$ samples A, B, and C.]

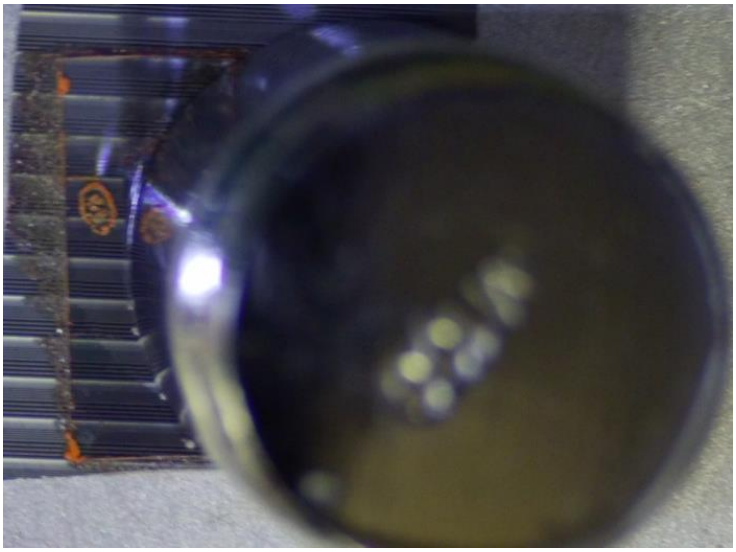
	Clamp Type	Hotplate Temp (C)	Anneal Temp (C)	Anneal Time (h)
Sample A	binder clip	80	80	48
Sample B	100g weight	80	80	48
Sample C	50g weight	80	80	72

We grew three samples according to Table 1 to compare the pressure distributions, one was held together with a binder clip, sample A and the other two were held together by a 100 g weight, sample B, and a 50 g weight sample C. With sample A

we noticed the crystals mostly grew in areas of higher pressure, i.e., around where the binder clip held the substrates together. In Figure 7 below we see crystal growth was localized to the areas around the binder clip. If annealed for a longer amount of time the crystals could have grown larger, with the limit being the amount of precursor solution available before the DMF evaporated.

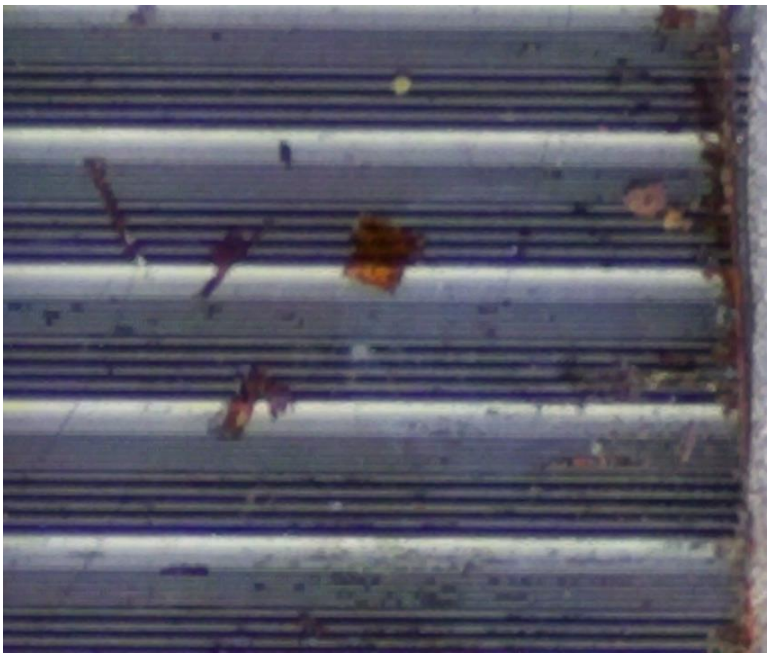


[Figure 7: $MAPBr_3$ crystal growth started near binder clip in sample A.]

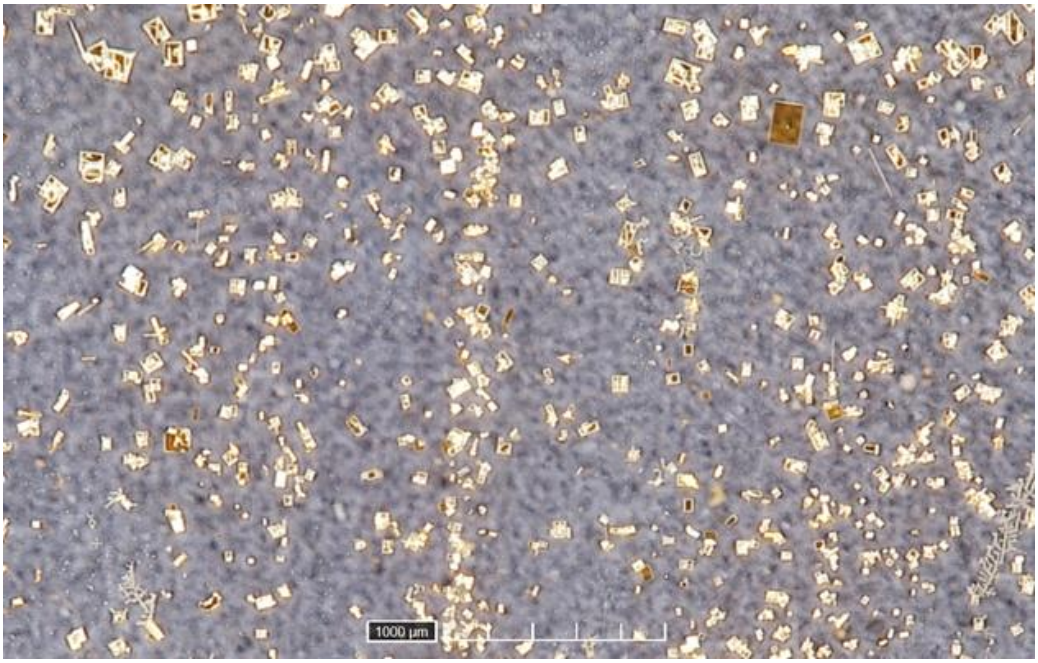


[Figure 8: 100 g weight holding sample B together.]

To apply the pressure evenly over the substrates we tried replacing the binder clip with a 50 g and 100 g weights, the 100 g weight set up is shown in Figure 8 above and the resulting crystals are shown in Figure 9, but the pressure provided by the weights was insufficient for patterned crystal growth as most crystals grew over the patterned substrate instead of throughout the trenches. Figure 10 shows the crystals from sample C that were grown under a 50 g weight, for an additional 24 hours, because upon first inspection of the sample before substrate separation, there were no crystals visible. The crystals in sample C were much smaller than the single crystals grown in sample B despite the extra annealing time, and the crystal growth did not follow the patterned substrate that well.



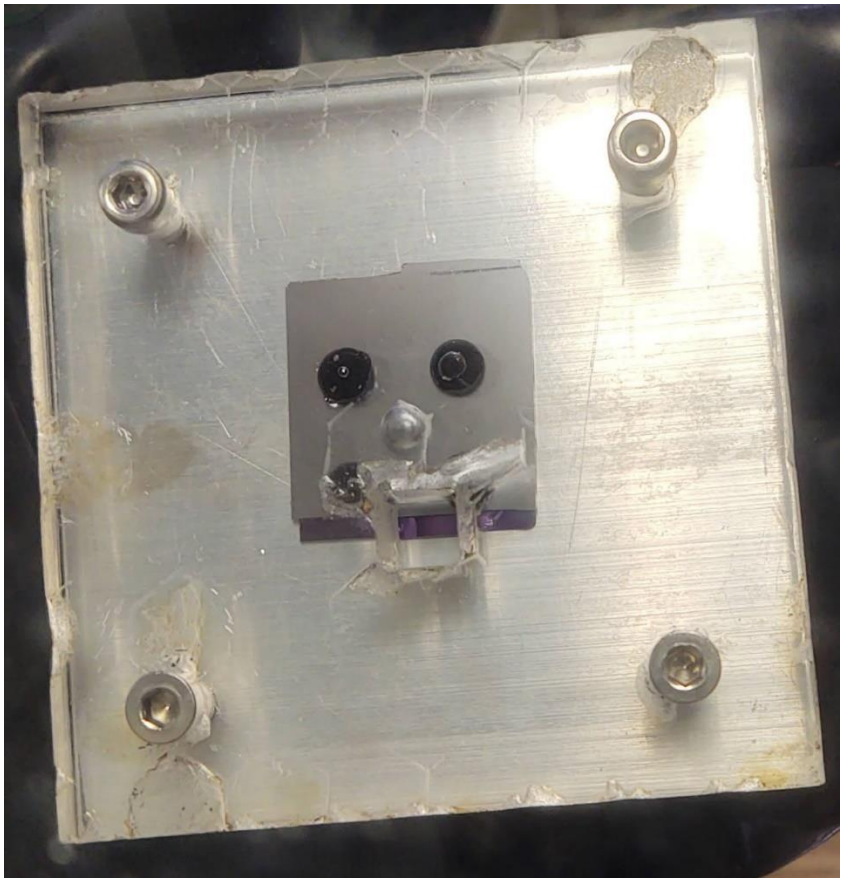
[Figure 9: Crystals grown in sample B under 100 g weight.]



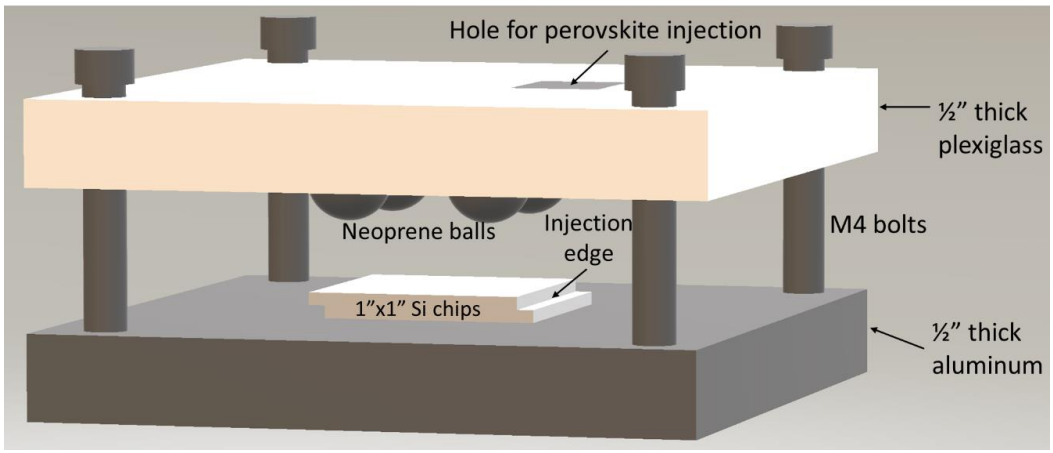
[Figure 10: $MAPBr_3$ crystals grown in sample B under 100 g weight.]

This is what drove us to make a custom clamp to apply adequate pressure evenly over the surface of the substrates as shown in Figures 11 and 12. The custom clamp consisted of a 3" x 3" x 1/2" aluminum block with screw holes in the corners cut and

threaded for M4 screws, and a 3" x 3" x 1/2" plexiglass block with holes just large enough for the M4 screws to slide through and screw into the aluminum block to hold the top and bottom together, as well as a hole to deposit the perovskite precursor solution on the sample. Additionally, to ensure the pressure spreads evenly, five-minute epoxy was used to secure 4 high strength neoprene rubber balls purchased from McMaster-Carr at the corners of a 1" x 1" square in the center of the clamp.



[Figure 11: Custom sample clamp holding two silicon substrates.]



[Figure 12: Custom clamp schematic.]

Substrate Patterning

There were three types of substrates used to create the two FET structures, all of which used 100 mm diameter p-type Si wafers with 0.001 – 0.005 $\Omega \cdot cm$ resistivity. One was a patterned substrate with trenches to promote capillary action and direct the single crystal growth. The other two were the contact substrates which followed the BC and TC FET structures. The BC substrate was coated with 200 nm of SiO_2 on average and was patterned with 85 nm Cr/Au contacts. The TC substrates were 100 mm Si wafers purchased from Graphene Supermarket and had a 285 nm thick SiO_2 layer and 0.001 – 0.005 $\Omega \cdot cm$ resistivity, the contacts were deposited through a shadow mask after the crystals were grown, and both silicon wafers were 500 μm thick.

To avoid surface contamination, we patterned our substrates in the Nanofabrication Research Service Center (NRSC) cleanroom's photolithography bay. We started with 100 mm diameter bare p-type silicon wafers 500 μm thick and spin-coated a positive photoresist (PR), KL5310, with a 2-step spin recipe detailed in Table 2, inside the Xanthos fume hood, which resulted in an average thickness of 1,366.4 nm $\pm$47.17 nm. They were then annealed at 100°C and exposed to ultraviolet (UV) light for

3s under a patterned photomask in hard contact mode in the contact aligner, then brought back into the fume hood to be annealed at 115°C. After 1 minute the wafers were placed back in the spin coater and developed in a puddle of 0.26 M tetramethylammonium hydroxide (TMAH) for 40 s then spun at 4000 RPM for 30 s. Then the pattern was checked under an optical microscope for PR in the areas that should have been exposed and washed away, because if there is residual PR left over the pattern will not translate into the wafer well. To remove residual PR, we exposed the wafers to oxygen based plasma in the PE50 O_2 plasma asher at 1000W power for 1–2-minute intervals, while checking under an optical microscope each time until the desired pattern was clear.

[Table 2: Spin coater parameters for photolithography.]

	Speed (RPM)	Time (s)	Average	UV
Step 1	700	5	Thickness (nm)	Exposure (s)
Step 2	780	70	1366.9	3

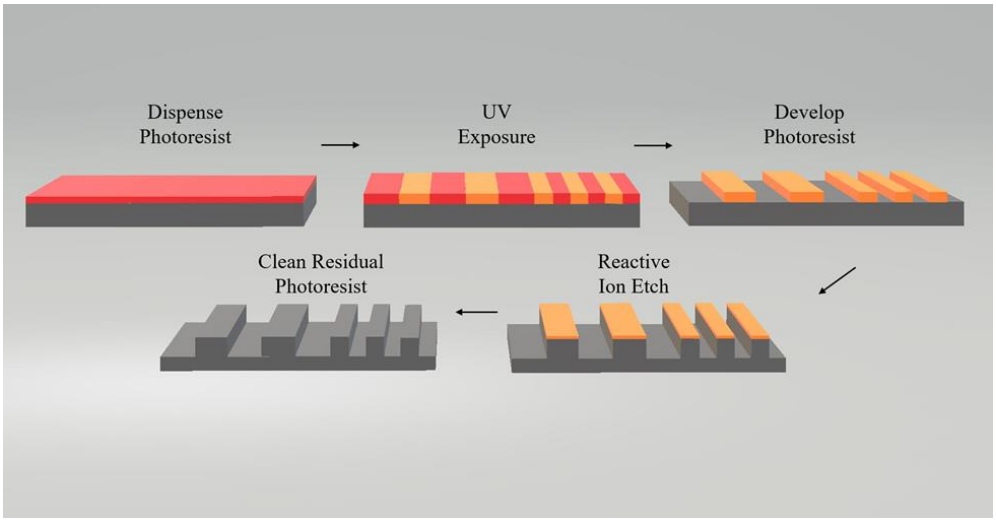
Next, the substrates were rinsed with deionized (DI) water to remove the exposed photoresist and create a striped pattern. The pattern we used on the photomask consists of stripes increasing in width with equal distance between them to create a hill and valley step pattern across the wafer, which increased in width from 1μm, 2 μm, 5 μm, 10 μm, 20 μm, 50 μm, and lastly 100 μm. The wafers were then dry etched according to the parameters in Table 3, in the Oxford inductively coupled plasma (ICP)/reactive ion etcher (RIE) to translate the pattern into the substrate, the target step height between the steps and trenches was 2.5μm, because the target thickness of the thin film spacers was 2.5 μm

.

[Table 3: Oxford ICP/RIE etching conditions.]

	Gas Flow (SCCM)			
ICP (W)	RIE (W)	Ar	SF6	Time (m:s)
800	80	5	45	1:30

The photoresist patterned wafers were exposed to 800/80 ICP/RIE for one minute and thirty seconds. After etching, the substrates were brought back into the Xanthos Hood's spin-coater to be cleaned of residual photoresist by dispensing Acetone, Methanol, and Isopropyl in that order while spinning the wafer at 2000 RPM, then blow dried with a dry nitrogen gun to try and ensure a dust free surface. Next, we checked the pattern's step height in the profilometer to make sure the target step height was reached, and then the wafers were cleaved into roughly 1" x 1" chips. This process is represented below in Figure 13, additionally these stripe-patterned chips are used in both BC and TC transistor creation to guide the perovskite solution and make the resulting crystal height more controllable.

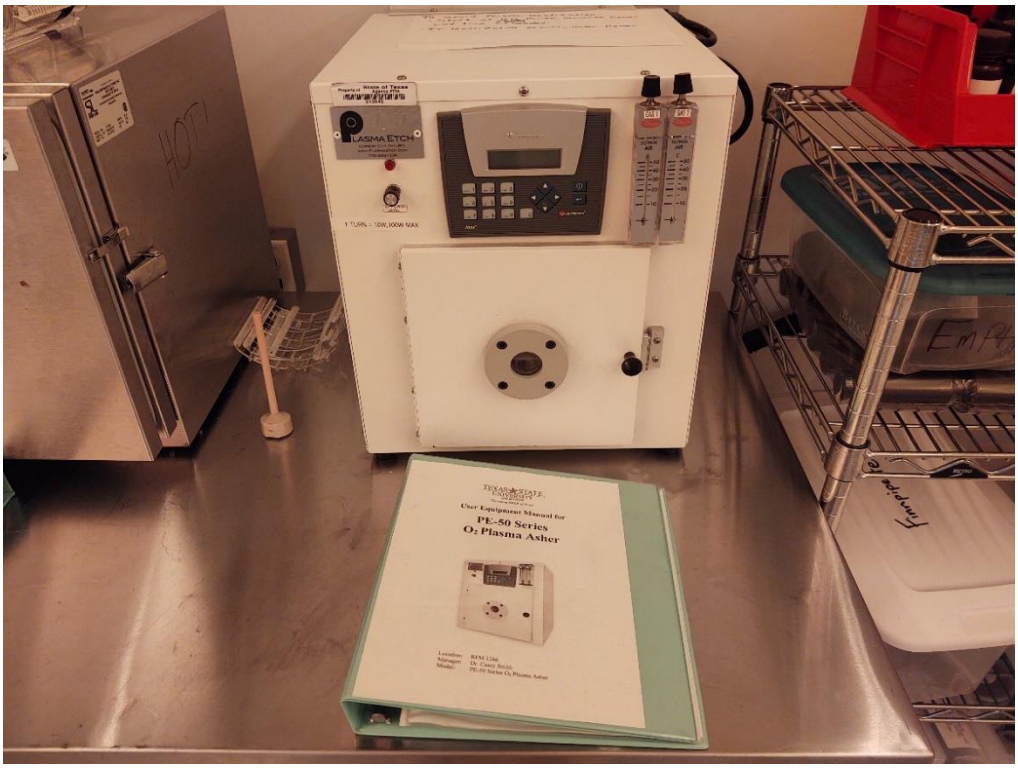


[Figure 13: Process flowchart highlighting patterned substrate creation.]

To make BC transistors we followed the process shown in Figure 14, starting with

the dielectric layer, we deposited ~200 nm of SiO_2 onto clean 100 mm diameter wafers using the NRSC wet oxidation furnace, pictured in Figure 14. The Si wafers were cleaned in the NRSC PE-50 O_2 plasma asher, shown in Figure 15. They were exposed to 50 W RF plasma for 1 minute prior to transfer to the wet oxidation furnace.

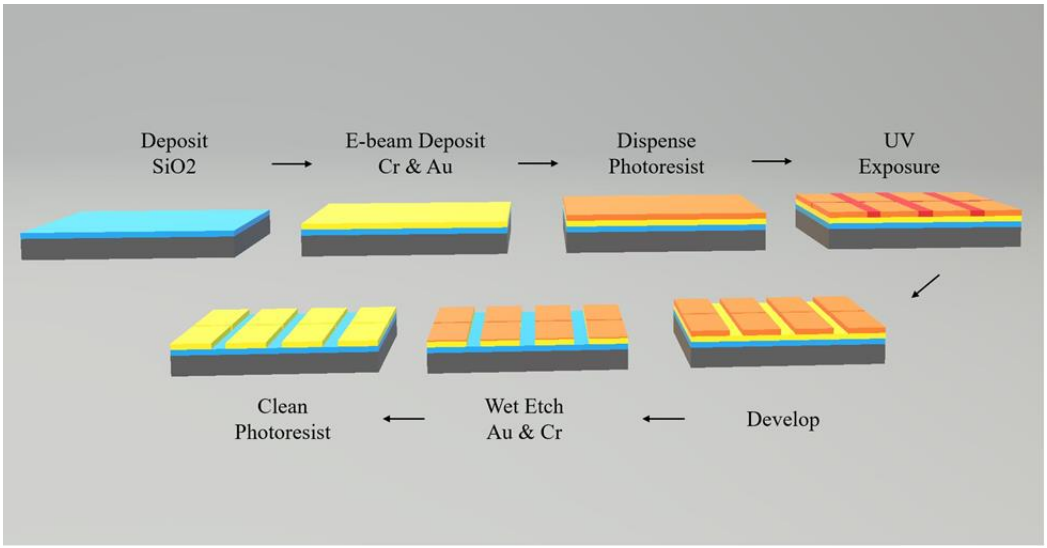
[Figure 14: Wet oxidation furnace with 100 mm diameter Si wafers.]



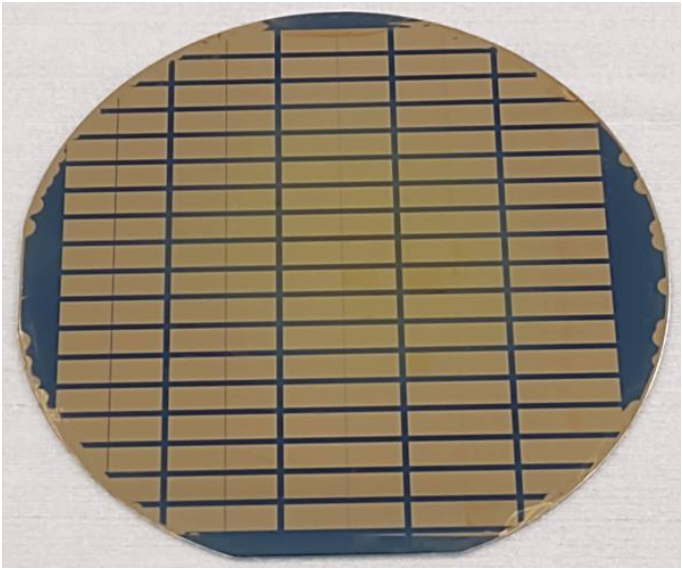
[Figure 15: PE50 O_2 plasma asher.]

Next, we used an electron beam evaporator to deposit 5 nm of chromium to act as an adhesion layer between SiO_2 and the subsequent deposition of 80 nm of gold. From here we followed a similar photolithography process to spin-coat and pattern photoresist on the gold surface to make the source-drain (SD) electrode's pattern. Except we used a different photomask to create the pattern for source-drain contacts, which had increasing channel length starting at 10 μm, 20 μm, 50 μm, 100μm, and ending with 150 μm. Instead of dry etching to translate the pattern, this time we used a separate fume hood dedicated to solvent use to wet etch the exposed gold and chromium areas. First the 100 mm diameter wafers were placed in beakers at room temperature and doused in standard Au etchant purchased from Sigma Aldrich. After 1 – 2 seconds the wafer was rinsed in a separate beaker with DI water and blow dried with a CO_2 air gun. Once the beakers were rinsed and the waste etchant was properly disposed of, this process was repeated for the

chromium layer using CR-9 etchant. Note that this layer is much thinner, 5 nm versus 80 nm, so 1 second or less is appropriate for the etching time. The result of this process flow represented in Figure 16, is an array of contacts, as seen in Figure 17, each contact being roughly 85 nm in thickness, 7.5 mm in width and 4 mm in length.



[Figure 16: Process flowchart highlighting source-drain contacts substrate creation.]

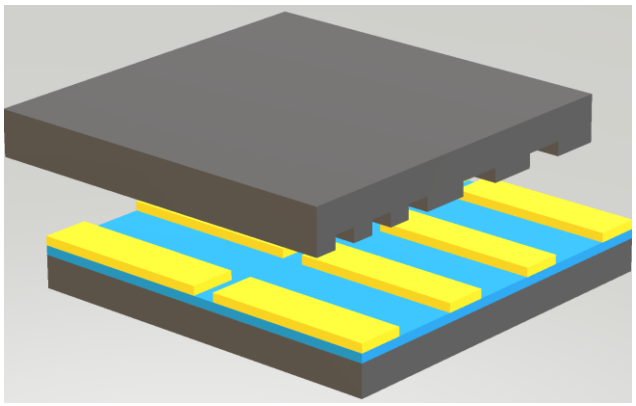


[Figure 17: SD contacts with channel length 150 μm, 100 μm, 50 μm, 20 μm, & 10 μm.]

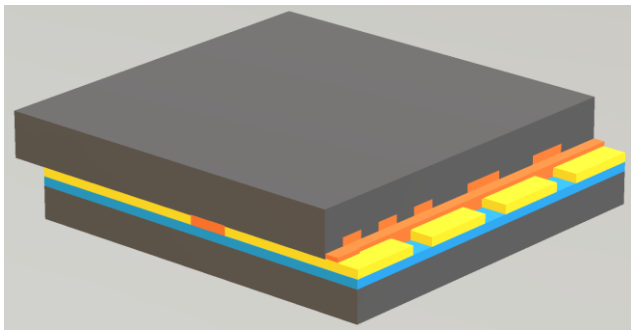
We decided to buy 100 mm Si wafers that were pre-coated in 285 nm of SiO_2

from Graphene Supermarket, because we had thickness inconsistencies between the center and the edge of the wafers that we deposited SiO_2 onto. Since the wafers from Graphene Supermarket arrived clean and individually packaged, all that was needed for TC substrate preparation was to cleave the wafers into chips as need.

Once the relevant substrate chips for the desired device architecture were cleaved, they were brought to Dr. Zakhidov's lab, cleaned in the RF plasma cleaner, and brought into a dry nitrogen glovebox for crystal growth. We clamped a patterned substrate with either a SD contacts substrate or a bare SiO_2 substrate for either the BC or the TC transistor structures respectively. However, in both cases, they must be clamped so that there is an edge to act as an entrance for the perovskite solution to be injected at, as shown in Figure 18 for a BC device. The striped pattern should always face the solution entrance in both BC and TC devices to promote capillary action in the trenches and avoid growing crystals under the hills of the patterned substrate. As mentioned in section 2.1, we used a custom clamp to improve the spread of the pressure during the annealing process. The downsides to this clamp design are that only one substrate can be annealed at a time, making sure each screw applies equal force, and too much force could cause the substrates to shatter in the clamp while annealing. Additionally, the ½" aluminum bottom required us to raise the temperature of the hotplate so that the temperature at the surface the sample sits on is the appropriate annealing temperature. To do so we used a digital multi-meter's thermometer and raised the temperature slowly until the surface temperature reached 80°C. In our case 85°C gave us our target temperature, but this could easily be affected by airflow and could require a higher temperature, especially if conducted in a fume hood instead of a glovebox.

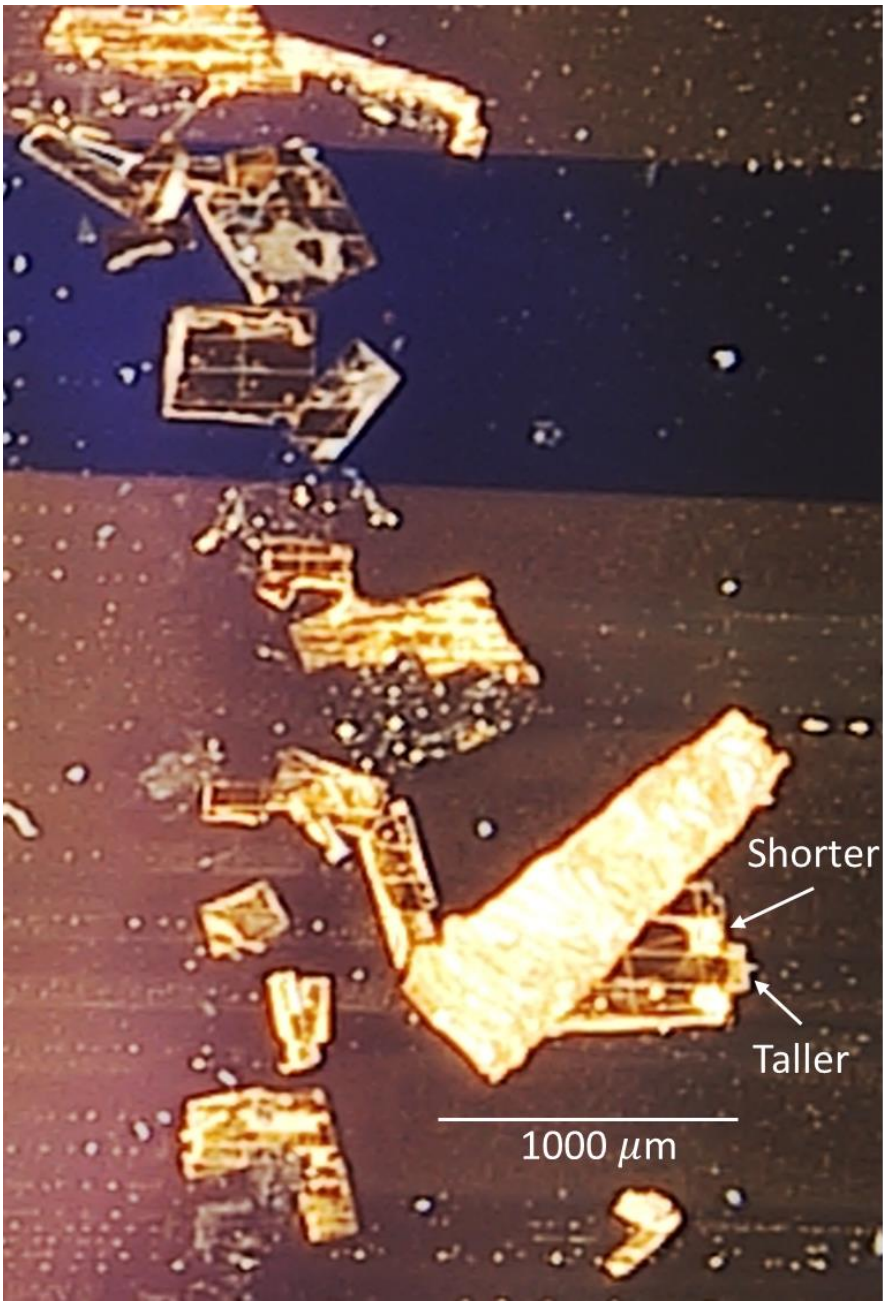


[Figure 18: Striped pattern clamped to direct single-crystal growth across SD channels.]



[Figure 19: $MAPBr_3$ perovskite precursor solution deposition.]

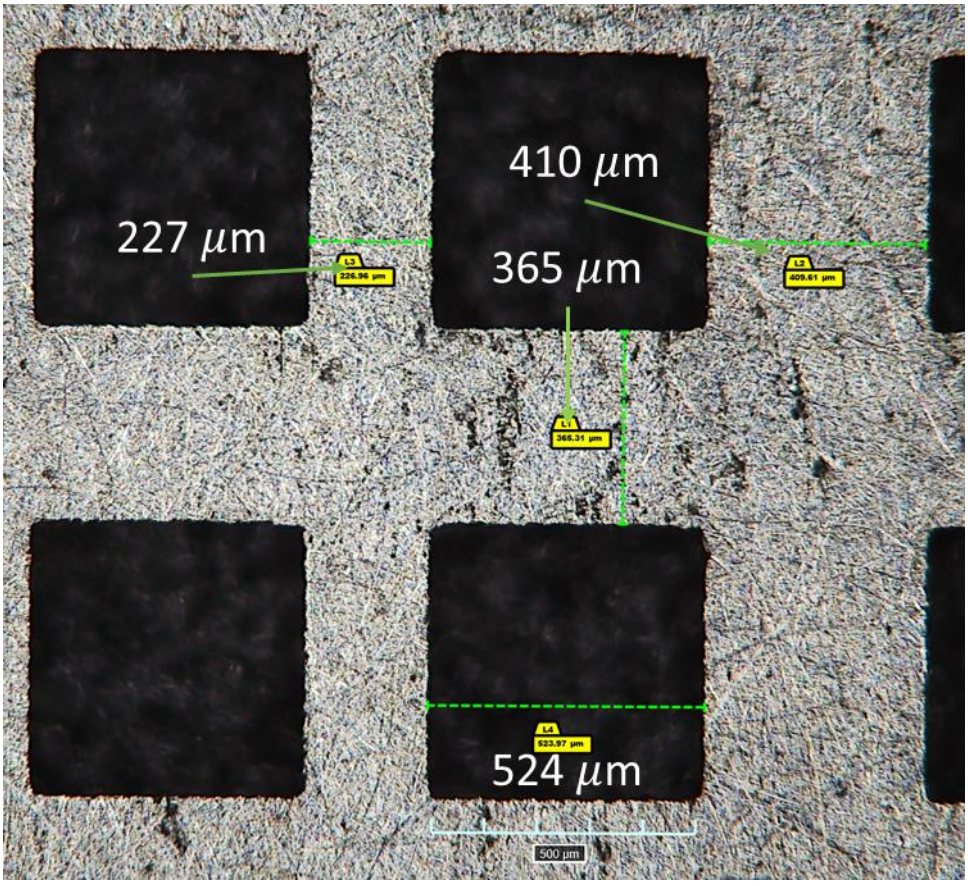
As depicted in Figure 19 above, the SD contacts substrate adds to the thickness where the crystals are allowed to grow. They are much shorter compared to the depth of the trenches, 0.085 μm versus 2.5 μm, but the increased thickness could affect the quality of crystal growth. Specifically, we noticed many crystals growing under both the hills and trenches, creating a step pattern in the crystals, shown in Figure 20, instead of a striped pattern.



[Figure 20: $MAPBr_3$ crystals grown across pattern in gap between SD contact pairs.]

To make a TC transistor the patterned silicon substrate is clamped with the 285 nm SiO_2 coated substrate, which is flatter than the BC contacts substrate so ideally there is minimal leakage across the striped pattern. The Cr/Au contacts are then deposited over the crystals after they are grown using a shadow mask in the electron beam evaporator.

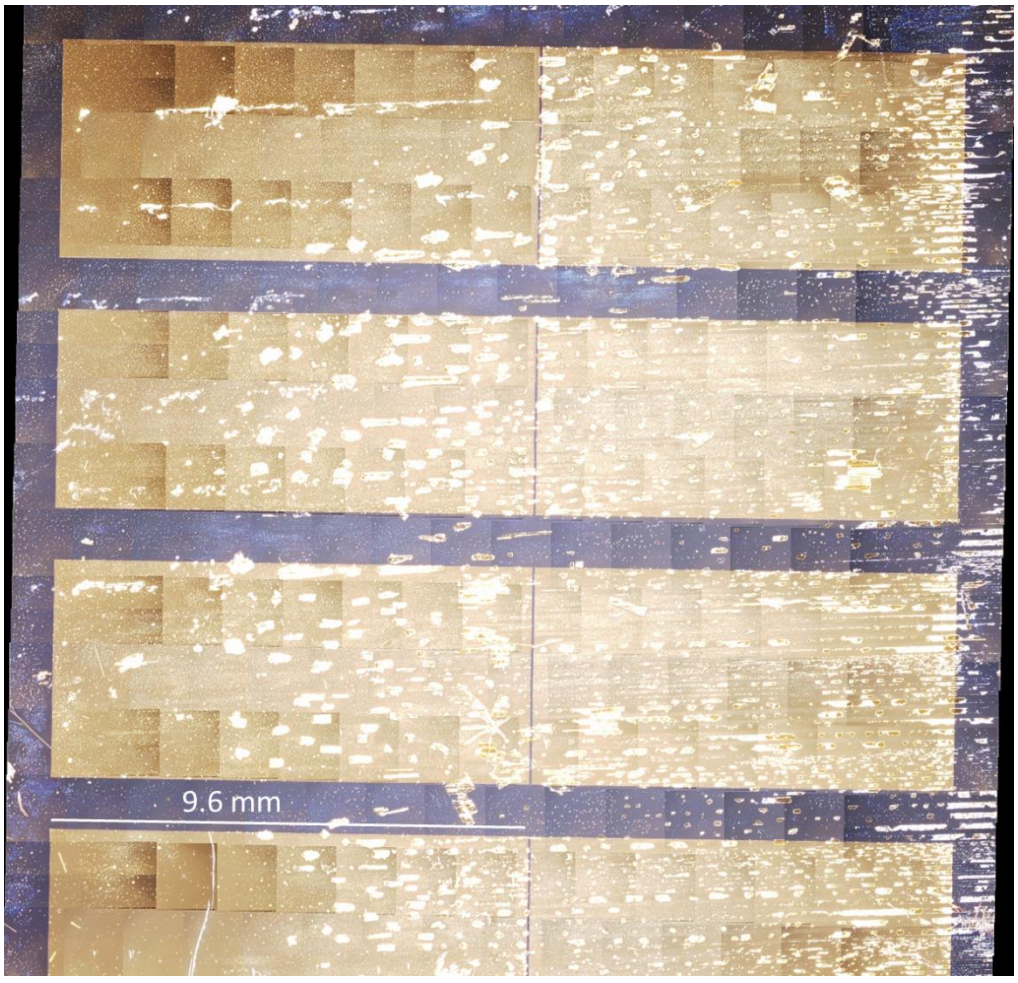
The shadow mask had 3 separate patterns with different channel lengths, from smallest to largest we had 130 μm, 230 μm, and 310 μm. Note the channel lengths here are much larger than those for the BC devices. This is due to the minimum cutting size set by the manufacturer of the shadow mask. Additionally, the target channel lengths were 100 μm, 150 μm, and 200 μm, but the manufacturer was limited by a minimum cutting size due to the thin metal warping from heat, leading to the larger channel length of 227 μm, shown in Figure 21. The smaller 100 μm channel length ended up being 131 μm, and the larger was 315 μm.



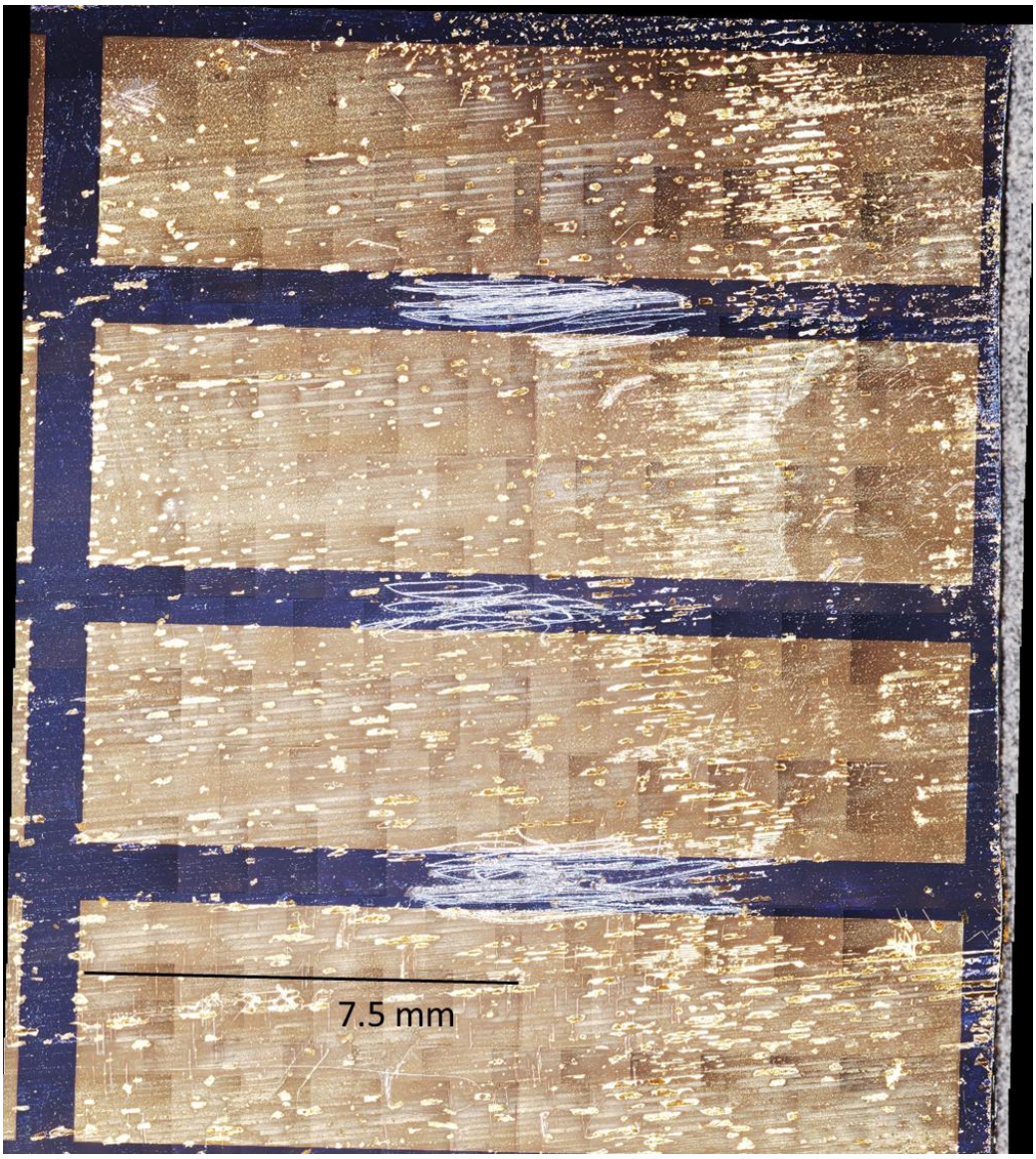
[Figure 21: Shadow mask for TC field-effect transistors.]

Few samples were coated in PTAA, because we realized the field-effect mobility could be influenced by this layer since it is conductive, and we wanted to find the field-

effect mobility of the perovskite. Plus, there was little difference in crystal growth between the two BC samples shown in Figures 22 and 23, which defeated the purpose of us including it in the device creation. Note the scratches seen in Figure 23 were to make contact with the gate before the copper plate method was implemented.



[Figure 22: BC FET that was cleaned with RF plasma and coated with PTAA.]



[Figure 23: BC FET that was only cleaned with RF plasma.]

Crystal Growth

The perovskite crystals are grown from a 1 molar methylammonium lead-tri-bromide, $MAPBr_3$ ($CH_3NH_3PbBr_3$), precursor solution. The solvent used to dissolve MABr and $PbBr_2$ together was N,N-Dimethylformamide (DMF), purchased from Sigma Aldrich. The solution mixing process is guided by a recipe made in Excel, to ensure the end solution is 1M. First approximately 440 mg of $PbBr_2$ was weighed out in a vial,

1,199 μL of DMF is added, and the solution is set to stir at 75°C until dissolved. Next approximately 114 mg of $MABr_2$ is weighed out in a second vial and 1,018 μL of solution from the first vial is added to the second vial, which is then set to stir at 75°C for 30 minutes.

Once the precursor solution was transparent and the solid materials are dissolved, 10μL of the precursor solution were injected at the sample entrance and drawn in-between the substrates via capillary action. The clamped sample is then annealed at 80°C for 2 days (48 hours). Note that the surface touching the sample needs to be 80°C, and with the use of our custom clamp the temperature of the hotplate's temperature was raised to 85°C, as mentioned earlier in subsection 2.1. If the annealing temperature is too low, then the DMF solvent may not evaporate, and the precursor solution will spread over the sample when the patterned and contact substrates are separated. After annealing, the substrates were separated, to expose the perovskite crystals for characterization.

After crystal growth and substrate separation the BC device is ready for characterization. However, the TC devices still required contacts, so we attached a shadow mask over the substrate and used the NRSC electron beam evaporator to deposit 5nm of chrome and 80 nm of gold. Care must be taken to directly apply and remove the shadow mask with minimal damage to the crystals.

Device Characterization

The crystal quality was characterized using optical microscopy, X-ray diffraction (XRD), scanning electron microscopy (SEM) and energy dispersive spectroscopy (EDS). Crystal thickness and roughness were measured using a profilometer and an atomic force microscope (AFM). Electrical characterization was done using 3 probes on the Cronus

four-point electrical probe-station.

Optical microscopy was carried out using the Hirox digital microscope from Figure 24. Images were taken using brightfield imaging which means the light illuminating the sample comes directly from the lamp with nothing to block its path to the sample. The magnification range of the microscope is 20x – 2500x, but most images were taken in the 20x – 160x range.

[Figure 24: Hirox digital microscope.]

To gather XRD data, X-rays of wavelength λ =0.154 nm, are collimated and directed at the sample. The rays interact with the atomic structure and leave the sample with a phase offset at certain angles. This creates diffraction interference peaks at certain angles in 2θ, relative to the X-ray's incident angle, θ. The measurement technique typically used for single crystals is parallel beam, where the incident X-ray beam is held

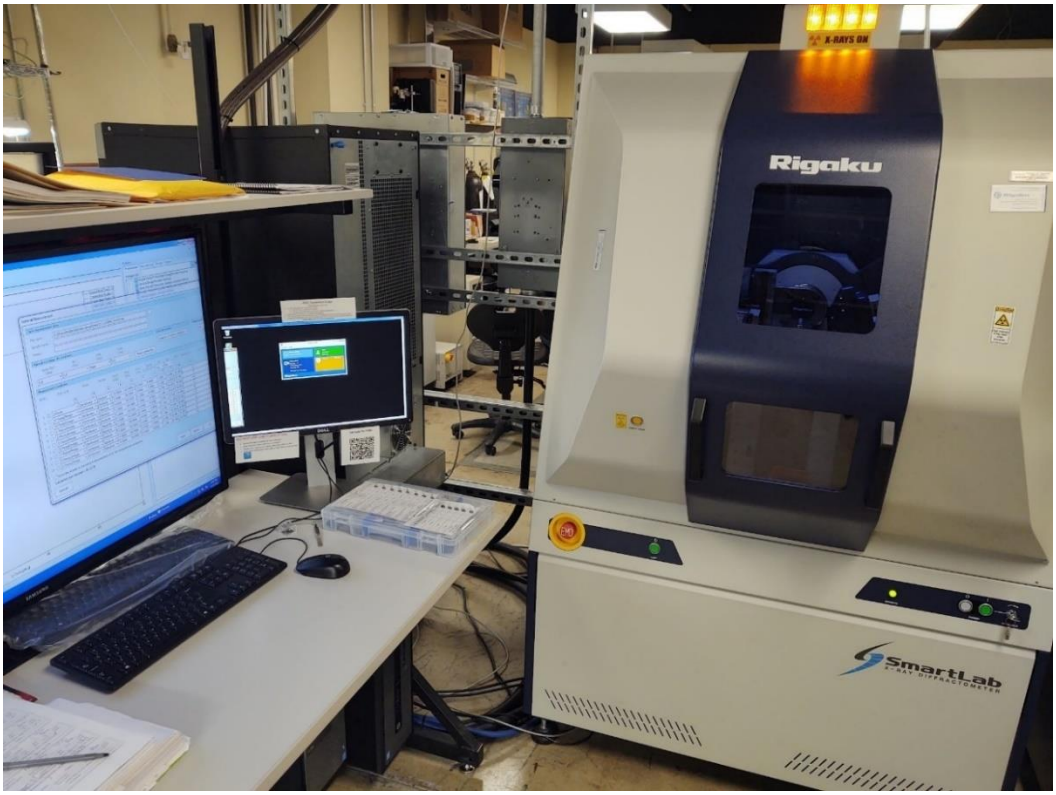
at a constant angle nearly parallel to the sample, and the receiving optics move through 2θ to observe the diffraction peaks. The parallel beam measurements made here were taken in a Rigaku Smartlab X-ray Diffractometer, shown in Figure 25, with the parameters shown in Table 4. $MAPBr_3$ single crystals are cubic, and we expected to see diffraction peaks at 2θ=15°, 30°, and possibly 46°, labeled (001), (002), and (003) respectively. The (003) peak may or may not be observed, Weili Yu. et al. reports the peak with similar intensity to the first two[8], but Wang et al. reports only the first and second peaks for $MAPBr_3$ single crystals[12]. The main issue with this measurement technique is the sample itself, if the crystal growth is too sparse, then the low chance of the X-ray beam landing on a crystal could result in non-relevant data. Typically, this was an issue observed in the samples held together with weights, because the crystals were both small and sparse, so the crystals covered little surface area of the substrate. We would also be able to calculate the thickness of the crystals we measure if they are nanometer scale. This is done by taking the full width at half the maximum (FWHM) value of a XRD peak and using it in Scherrer's equation.

$$\tau = \frac{\kappa\lambda}{\beta \cos(\theta)}$$

Here κ is the shape factor which is dimensionless and in the case of cubic perovskites, we can approximate $\kappa = 1$, λ is the wavelength of the incident X-ray beam, which is 0.154 nm for a Cu K-α X-ray source. The FWHM is represented by β, which must be converted to radians, and θ is the location of the XRD peak in 2θ divided by 2. However, most of the crystals we grew had a thickness on the micron scale.

[Table 4: XRD measurement parameters.]

	Incident beam			
	length limitng slit	2-theta range	Scan speed (°/min)	Step Size (°)
Sample D	2 mm	10 - 50°	1	0.01
Sample E	2 mm	10 - 50°	2	0.01



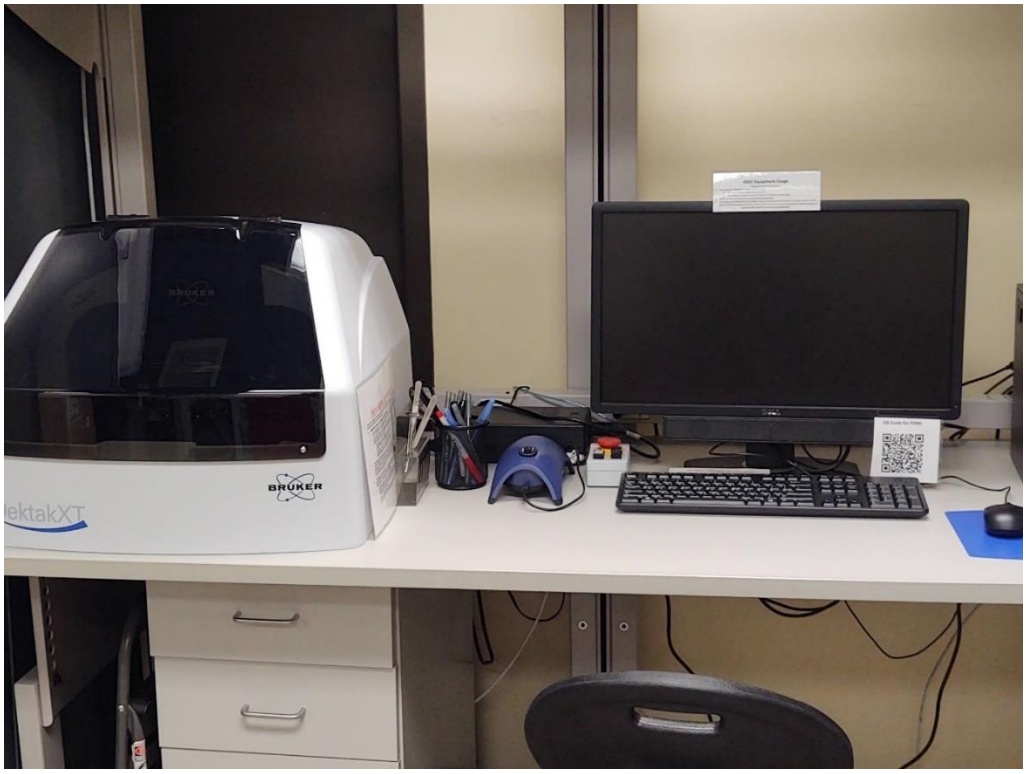
[Figure 25: Rigaku Smartlab X-ray Diffractometer.]

The SEM used was the Helios Nanolab 400, pictured below in Figure 26. To record images the SEM accelerates electrons down to the sample using a magnetic lens to focus the beam. Once the electrons collide with the sample X-rays are released and the electrons are scattered, then detectors record and combine the X-rays, backscattered electrons, and secondary electrons to form the final image. To use the SEM, the sample was grounded to a sample puck with copper tape to prevent charge build-up while imaging the crystals. SEM imaging can be destructive, so we first focused on areas near

the edge of the sample then moved to more interesting areas. We used a 10 kV accelerating voltage, and while looking around the sample we used 5 – 10 pA for the current to avoid damaging the sample. To take SEM images of areas of interest we increased the current up to ~21 pA, the sample must be grounded. We also performed EDS using the scanning electron microscope to do point analysis and make elemental maps of the crystals. Some crystals had areas around them with extra material, and these EDS techniques were used to check what the material was.

[Figure 26: Helios Nanolab 400 SEM.]

Profilometry was done using a Bruker DektakXT Stylus Profilometer shown below in Figure 27. This machine applies a 3 mg force and drags a tip with a 2 μm radius across the sample to measure step height and surface roughness in a line on the sample, creating a line profile.



[Figure 27: Bruker DektakXT stylus profilometer.]

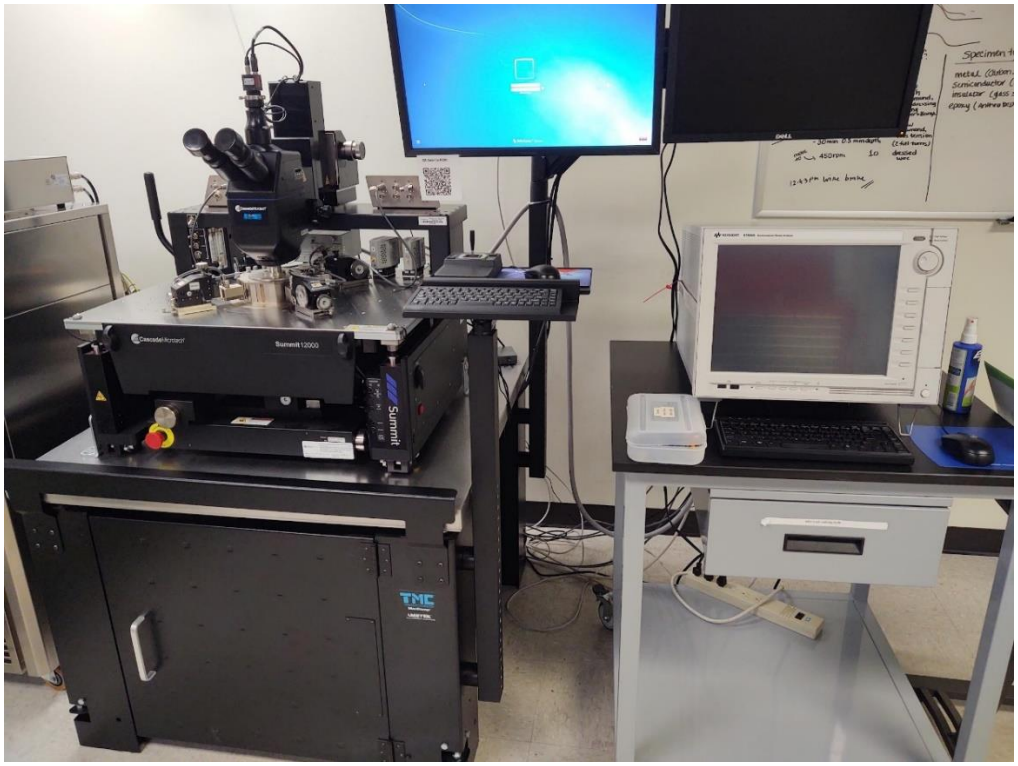
To measure the roughness of the crystals we used a probe tip with specifications from Table 5 in the Bruker Dimension Icon AFM from Figure 28. To avoid damaging the crystals we used soft tapping mode, which vibrates an 8 nm sharp tip at a resonant frequency of 160 kHz to lightly tap the sample and map the topography as changes in the oscillation amplitude are detected and corrected with a z-sensor. The tip oscillates at this frequency due to a cantilever that has a force constant of 5 N/m, and the dimensions 125 μm x 25 μm x 2.1μm. After data collection the AFM images were processed in an open-source software called Gwyddion.

[Table 5: Probe tip parameters used for tapping mode characterization.]

	Resonant	Cantilever	Reflective
Tip radius:	Frequency (kHz):	Force constant:	Coating:
8 nm	160	5 N/m	backside, Al

[Figure 28: Bruker Dimension Icon AFM.]

The electrical characterization was conducted with a Cronus 4-point probe station shown in Figure 29. The substrates were first scratched with a diamond scribe on the backside to expose bare silicon. Then silver paste was applied over the scratched surface and the substrate was placed on a copper plate to act as a gate contact for the probe station.



[Figure 29: Cronus 4-point probe station.]

III. RESULTS

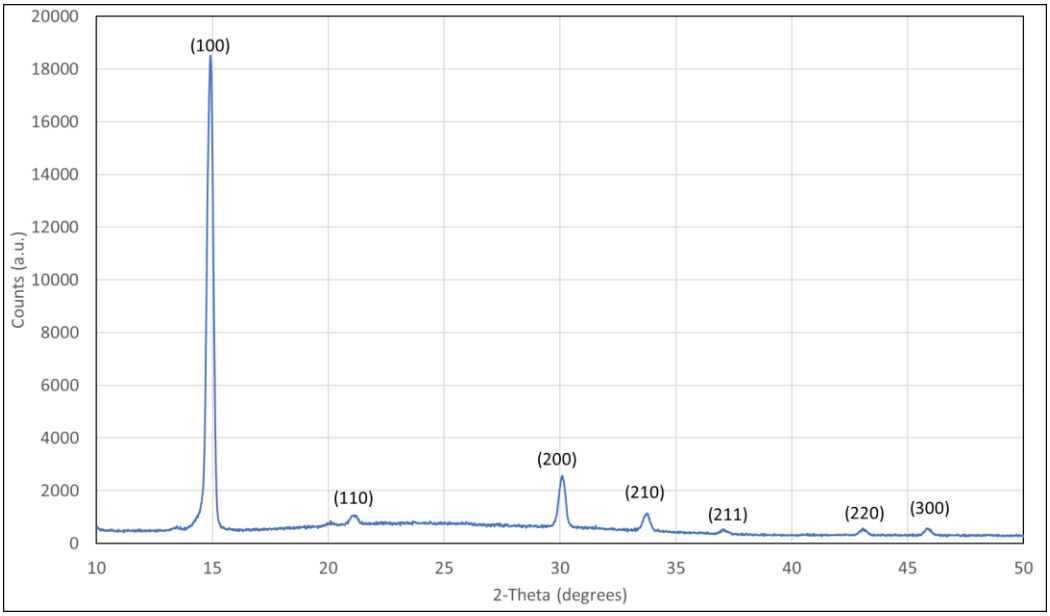
Crystal Quality

As stated in the crystal growth section we expected to see the XRD peaks (100) at $2\theta = 15°$, (200) at $2\theta = 30°$, and (300) at $2\theta = 46°$ if present for our single crystal sample. We used a 2 mm incident slit to narrow the X-ray beam, because the crystals are small and didn't cover the surface of the entire chip, so a narrower beam reduces the chance of observing multiple crystals which could have different orientations, but the intensities of observed peaks are relatively low. We spin-casted polycrystalline $MAPBr_3$ on glass at 4000 RPM for 60 seconds, then annealed the sample for 10 minutes at 80°C, to compare the XRD data with our single crystal data. As expected, the polycrystalline data in Figure 30 below showed more peaks than the single crystal's diffraction peaks. The XRD data in Figure 31 shows the expected (100) and (200) peaks, suggesting that single crystals were grown, but the ratio of the peaks suggest that more than one crystal was measured. We also see a very low and wide background peak around $2\theta = 24°$ from the glass substrate. We saw very little noise in the measurements with Si substrates but notice the difference in peaks observed between Figure 30 and 31. These two measurements were taken from two different samples, sample D and sample E, both of which were $MAPBr_3$ crystals, and their crystal growth conditions are listed in Table 6. We didn't observe the (300) peak for sample D, but a sample E which was made using the same clamp gave us not only the (300) peak, but a (210) peak at 2θ=34°. Sample D had larger crystals than the second, so it is likely that the X-ray beam covered more than one single crystal which were in different orientations for sample E, resulting in the smaller peaks shown in Figure 32. This difference in crystal size could also explain the

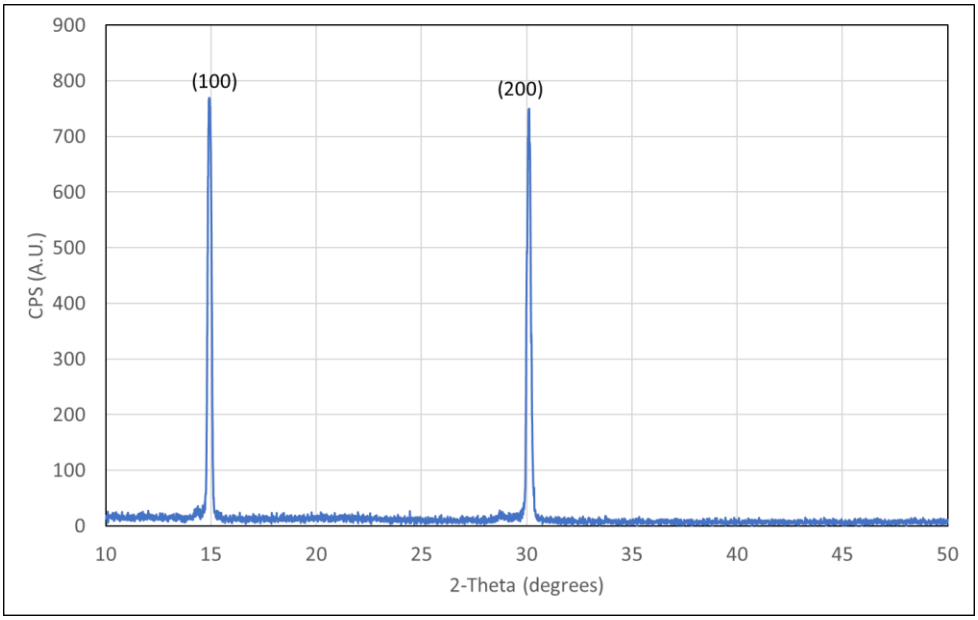
difference in intensity between the two sample's data. Smaller crystals cover less surface area of the substrate and contribute less scattered X-rays for collection.

[Table 6: Annealing conditions for $MAPBr_3$ samples D and E.]

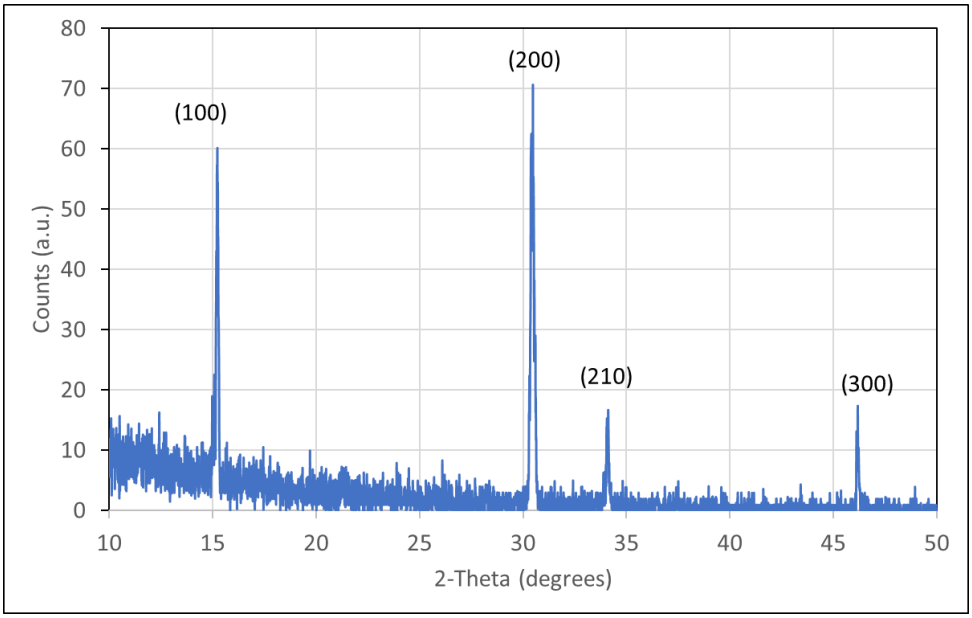
	Clamp Type	Hotplate Temp (C)	Anneal Temp (C)	Anneal Time (h)
Sample D	Custom	85	80	48
Sample E	Custom	85	80	48



[Figure 30: XRD data of polycrystalline $MAPBr_3$ spun on glass.]



[Figure 31: XRD data of $MAPBr_3$ single crystals from sample D.]

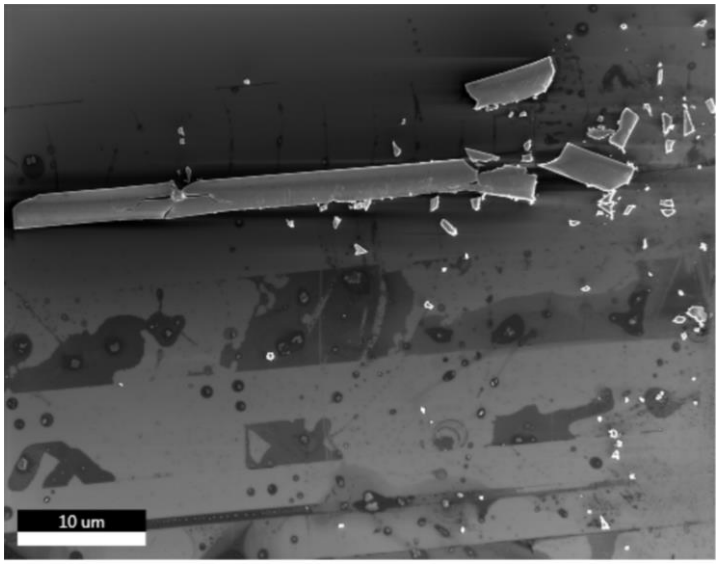


[Figure 32: XRD data of $MAPBr_3$ single crystals from sample E.]

As mentioned in the methodology of the XRD, we can use the Scherrer equation to calculate the thickness of nm scale crystals, since the single crystal thickness was a micron or larger on average we can't calculate the thickness. However, we can compare the two data sets, in Figure 31 we only see the (100) and (200) peaks and they are

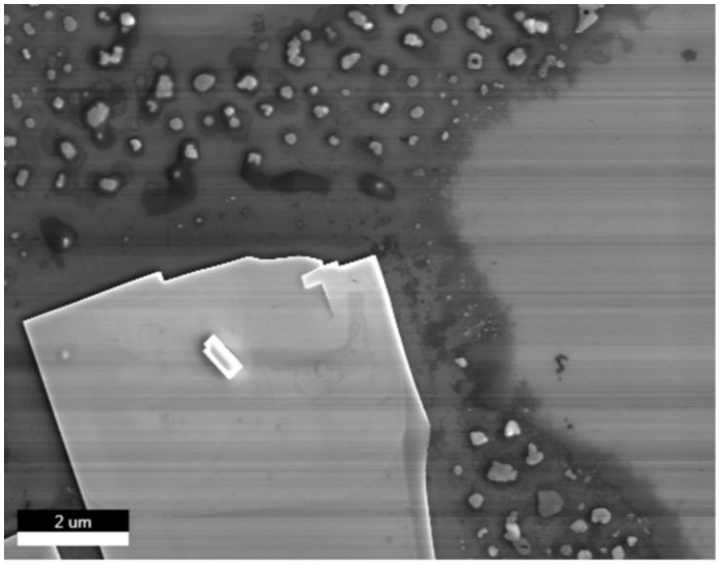
relatively the same intensity, suggesting more than one crystal was measured by the XRD beam, because the (200) peak would have a much smaller intensity than the (100) peak if only one crystal was measured. The XRD data of sample E from Figure 32 shows both (100) and (200) peaks suggesting multiple crystals were measured as well, but we also see the (210) and (300) peaks. From these two data sets we can conclude that there is a preferred crystal orientation for SiO_2 substrates, because the (100) and (200) peaks were both represented in the data. Additionally, there could be more than one preferred orientation since we saw the (210) and (300) peaks with smaller intensity. For the polycrystalline XRD data from Figure 30, we can use Scherrer's equation. These XRD peaks had a FWHM of $\beta = 0.0056\, rad$ and $\beta = 0.0072\, rad$ for the (100) and (200) peaks respectively, using these in Scherrer's equation we find $\tau_{(100)} = 27.81\, nm$ and $\tau_{(200)} = 22.29\, nm$.

The SEM image in Figures 33 below shows $MAPBr_3$ crystals from Sample D. There are no visible grain boundaries, which supports our earlier conclusion from the XRD data that these are single-crystal $MAPBr_3$ perovskites. Note the "shattered" look on the crystal stripe in Figure 33, this could be a result from separating the two substrates after annealing, which could negatively affect device reproducibility.

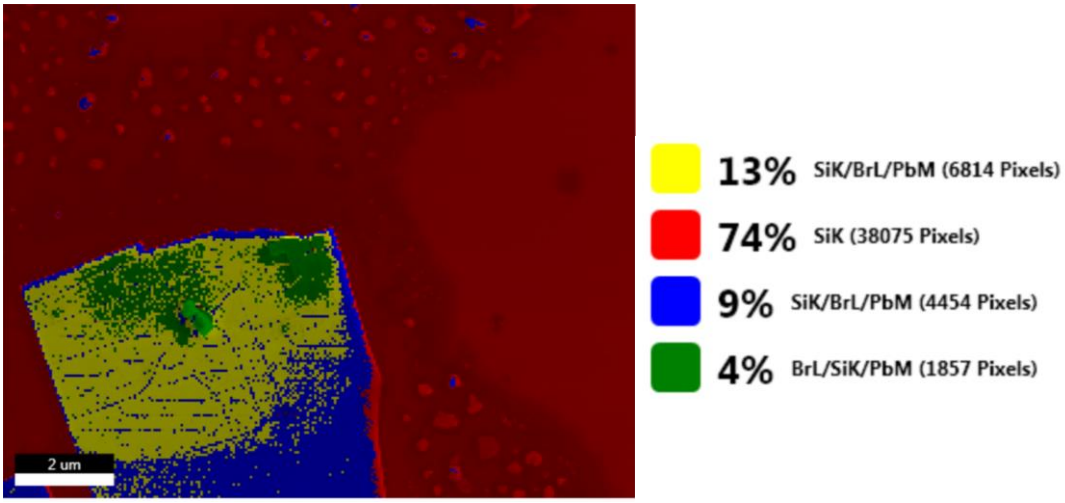


[Figure 33: $MAPBr_3$ grown along striped pattern.]

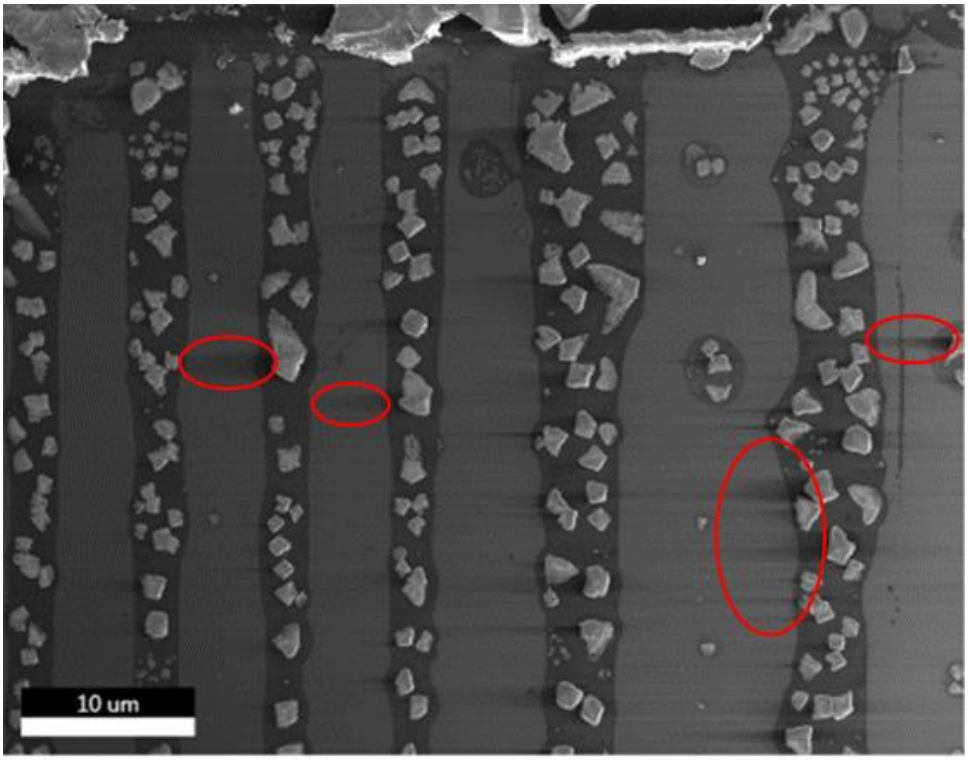
In Figure 34 below, we see a single crystal from sample D that didn't follow the pattern during growth, and there appears to be the start of a grain boundary in the corner of the crystal. Since the four corners of the substrates are held down by rubber balls, the center of the sample could have less pressure which could explain why this crystal didn't follow the pattern. Additionally, there are left over materials in a shadow surrounding the crystal. The shadow was too thin to observe in the elemental map shown in Figure 35, it could be component materials like CH_3NH_3Br or $PbBr_2$ which would explain the darker shadows surrounding some of the smaller crystals in Figure 34. From Figure 36 below, we can see the difference in crystal size and number between the two samples shown in the XRD data, supporting the idea that the X-ray beam covered more than one crystal that grew in different orientations.



[Figure 34: $MAPBr_3$ that didn't follow pattern.]



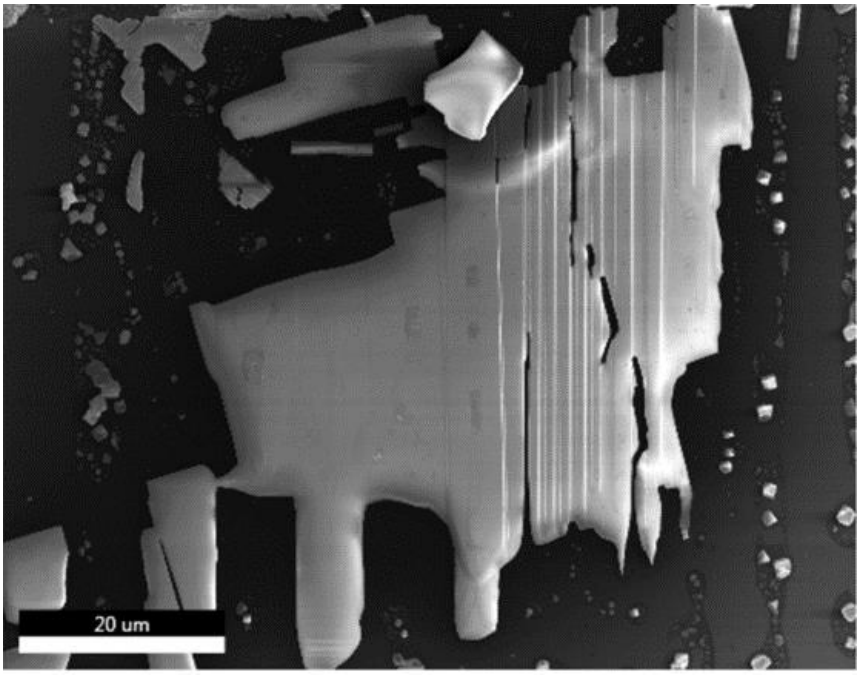
[Figure 35: $MAPBr_3$ elemental map.]



[Figure 36: $MAPBr_3$ small single crystals grown in stripes of sample E.]

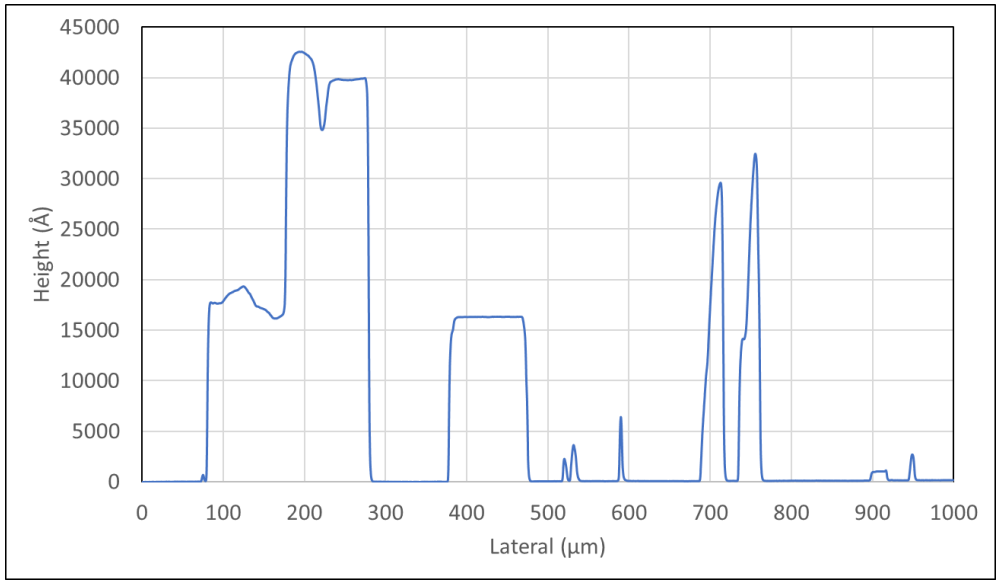
Figure 36 above is an SEM image from sample E that shows the difference in crystal sizes, the average width of these smaller crystals was 1.43 μm versus the larger crystal that was about 7 μm wide and the crystal stripe which was bout 30 μm long. The possible differences between samples D and E, are the pressure applied during the annealing process, and the space between the patterned and SiO_2 substrates. Figure 37 shows a much larger single crystal that could have increased the space between the substrates while other areas of the sample were annealing, causing the solution to leak under the pattern and allow smaller crystals to form in separate orientations. This growth pattern could be the result of one bolt applying more force than the other three causing an uneven pressure distribution on the sample. Additionally, note the dark streaks coming from some of the crystals circled in Figure 36, this is believed to be an artifact of the crystals charging during imaging, because while the sample was grounded with copper

tape, these crystals grew in a disconnected fashion on top of SiO_2 which is an insulating material.

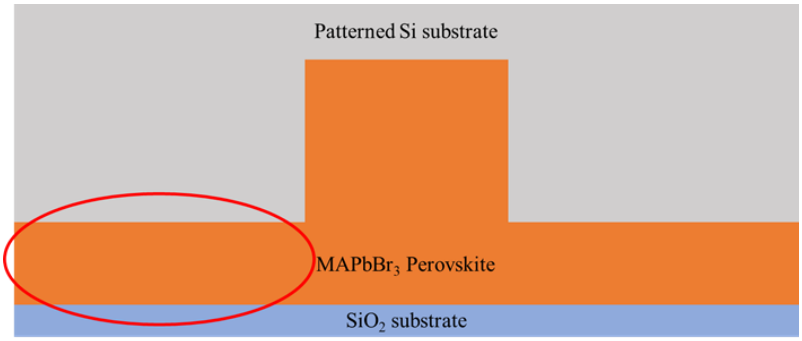


[Figure 37: Large crystals that expanded the distance between substrates of sample E.]

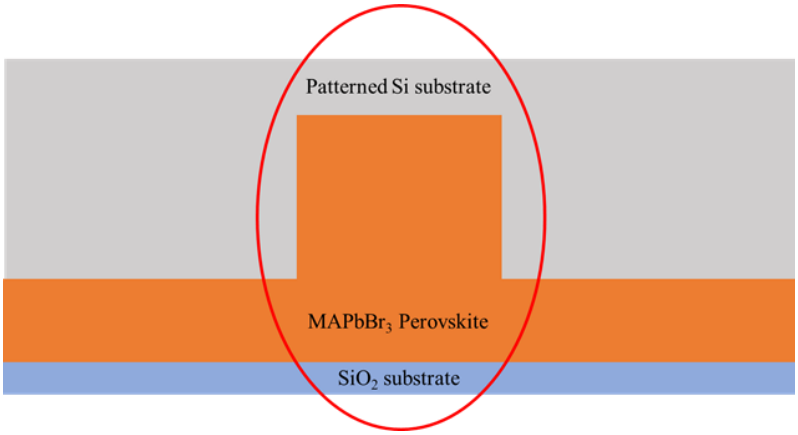
The step height of our crystals measured in the profilometer further explains why the other areas seemed to not have enough precursor solution. As can be seen below in Figure 38, the crystals that grew under the hills of the striped substrate, depicted in Figure 39, were about 1.5 μm tall. The crystals that grew in the trenches of the pattern, illustrated in Figure 40, were ~ 4 μm tall, the total difference in height is 2.5 μm, suggesting that single crystals grew in the pattern and continued to press the substrate upward. This ultimately increased the space between the substrates and allowed the crystals that had begun forming to grow taller instead of growing wider and connecting with one another.



[Figure 38: Profile of $MAPBr_3$ single crystals on SiO_2.]



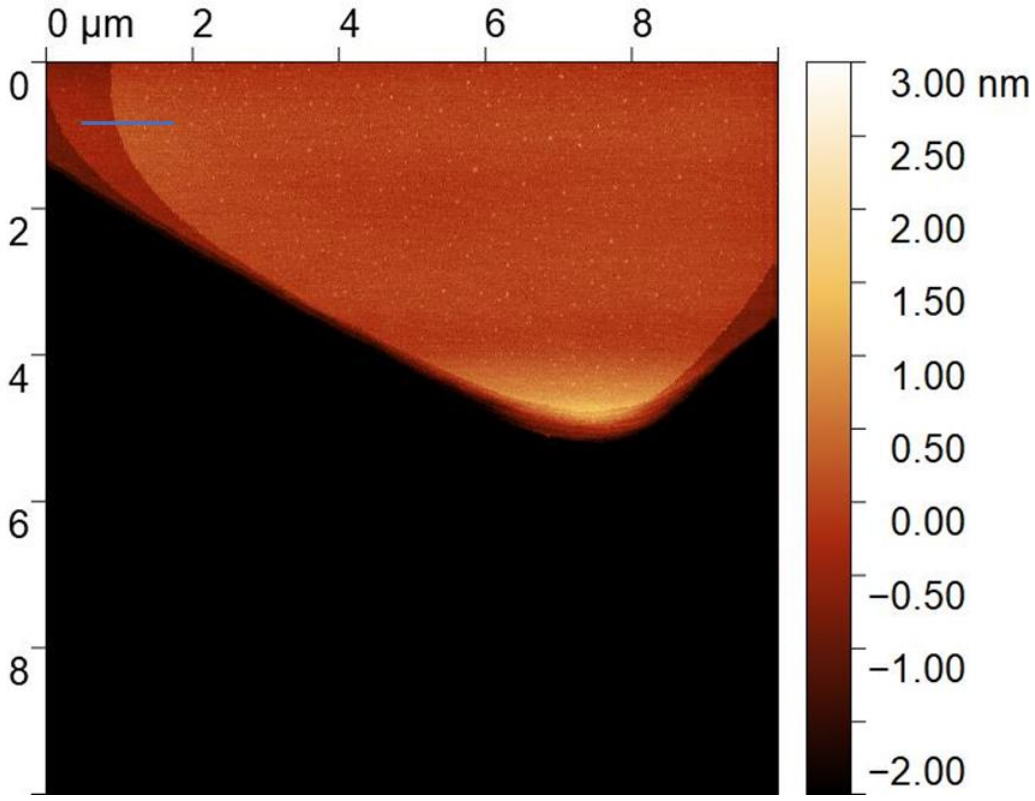
[Figure 39: Crystals grown "under hill" of patterned substrate.]



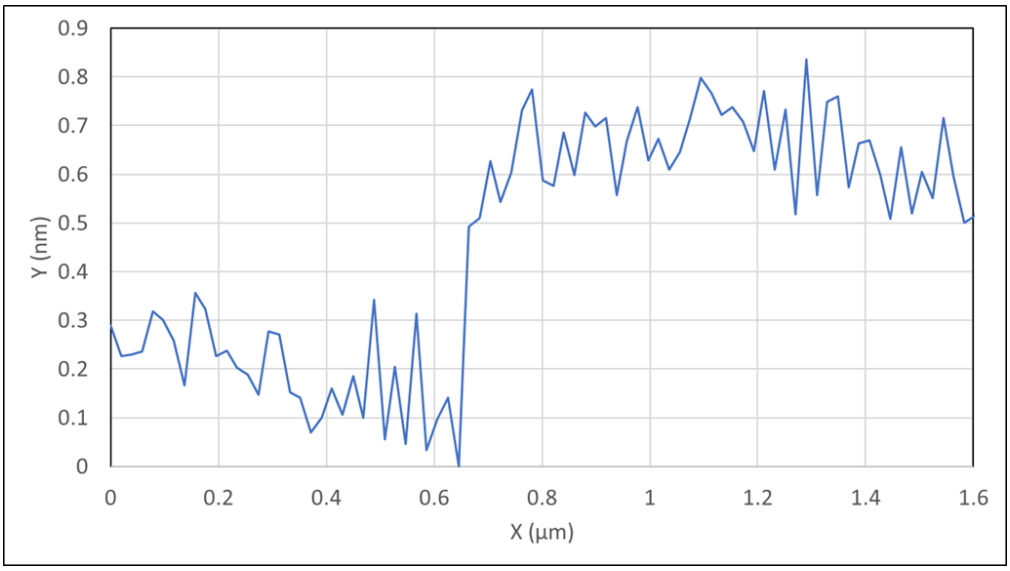
[Figure 40: Crystals grown "in trench" of patterned substrate.]

While roughness can be calculated with the surface profilometer, we used a

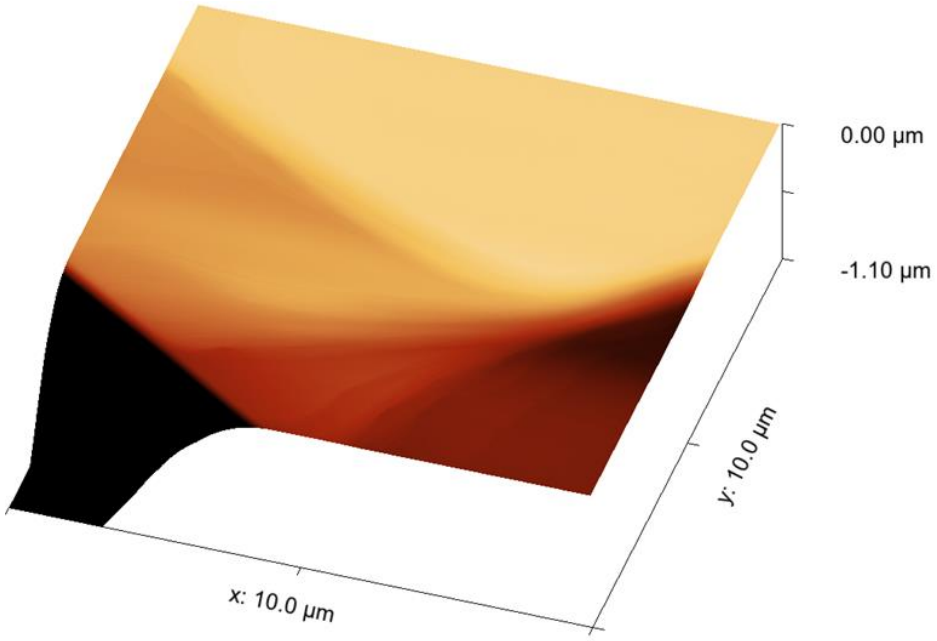
Bruker AFM for more accurate measurements since the tip radius is smaller than the profilometer tip. Some crystals grown were atomically flat as seen in Figure 41, with a root mean square (RMS) roughness of 139.3 pm. Figure 42 shows the profile of the steps seen at the edge of the crystal which is consistent with the reported lattice constant 0.59062 nm[9], showing an atomic step. Figure 43 shows a 3D perspective of the same data selected to display many similar steps along the edge of the crystal.



[Figure 41: Smooth crystal with 139.3 pm RMS roughness.]



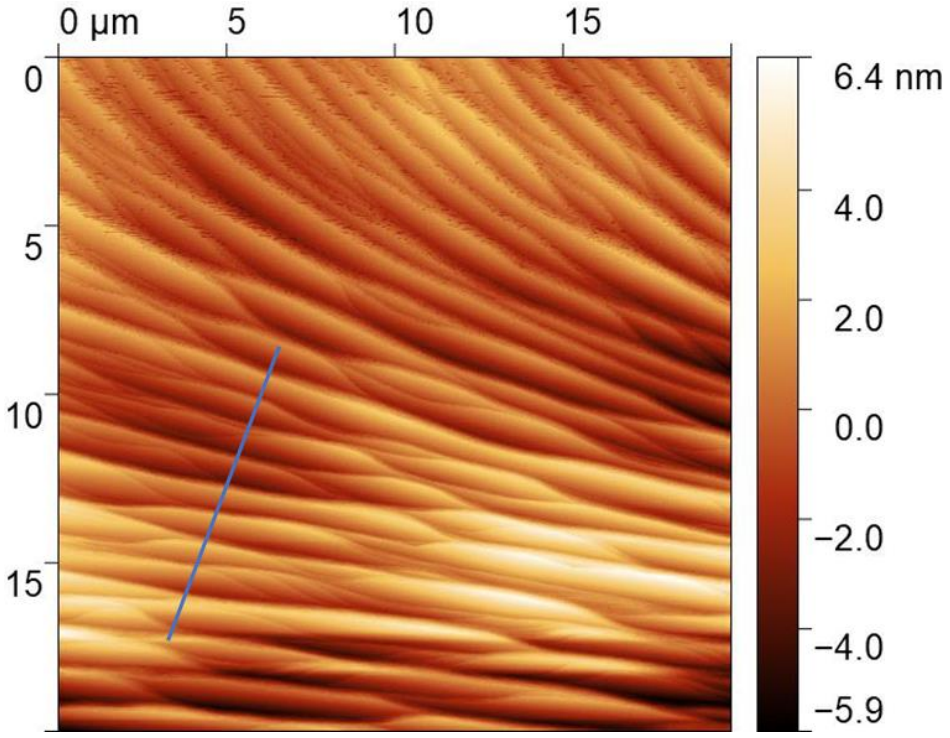
[Figure 42: Line profile showing atomically flat $MAPbBr_3$ crystal with a single monoatomic step.]



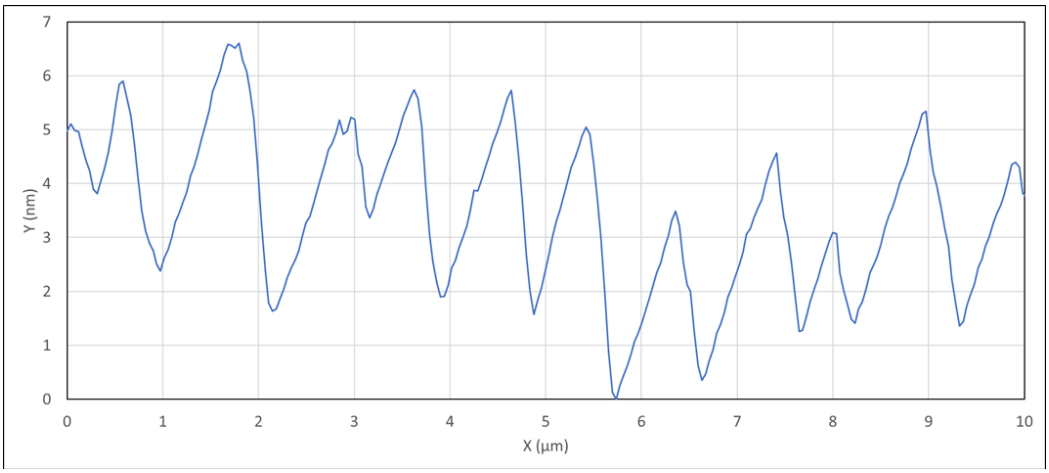
[Figure 43: 3D view of flat crystal.]

The surface of a crystal that grew in the trench of the patterned substrate was terraced as seen in Figure 44, with a RMS roughness of 1.73 nm. This could be a result from cleavage during separation of the substrates, or it could mean the crystals didn't

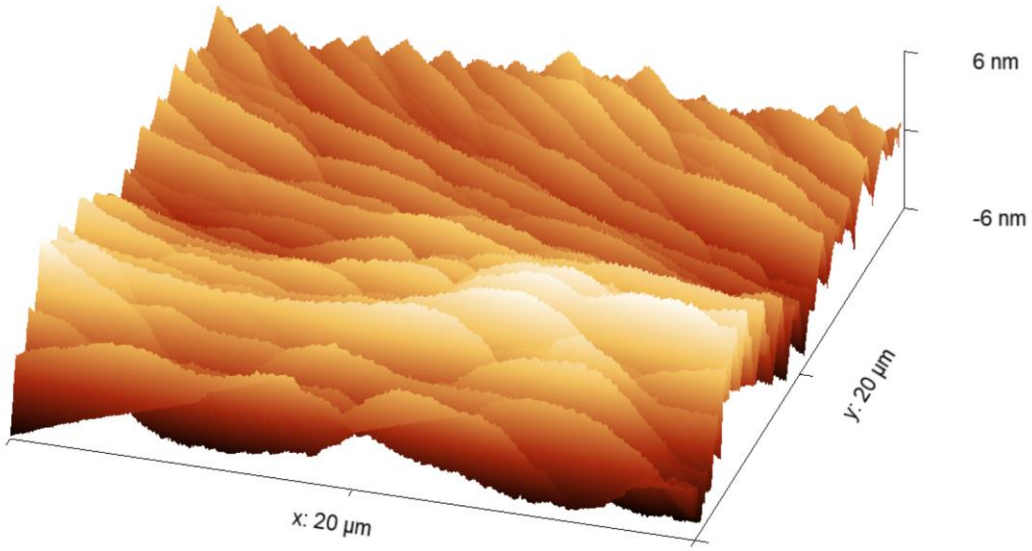
grow tall enough to fill the trench of the patterned substrate and were oriented so that steps came out at the top of the crystal. The profile shown in Figure 45 shows the steps are larger than the 0.59062 nm lattice constant determined by Shen et al.[9] so it is likely that the crystal was cleaved when the patterned substrate was removed. Figure 46 is the 3D representation of this crystal surface.



[Figure 44: Crystal grown in trench with RMS roughness 1.73 nm.]

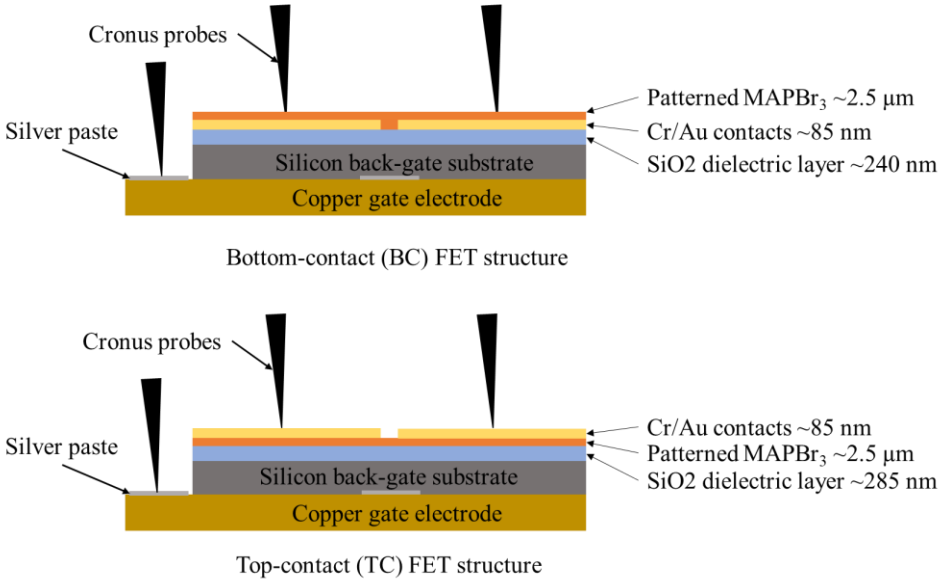


[Figure 45: Line profile of $MAPbBr_3$.]



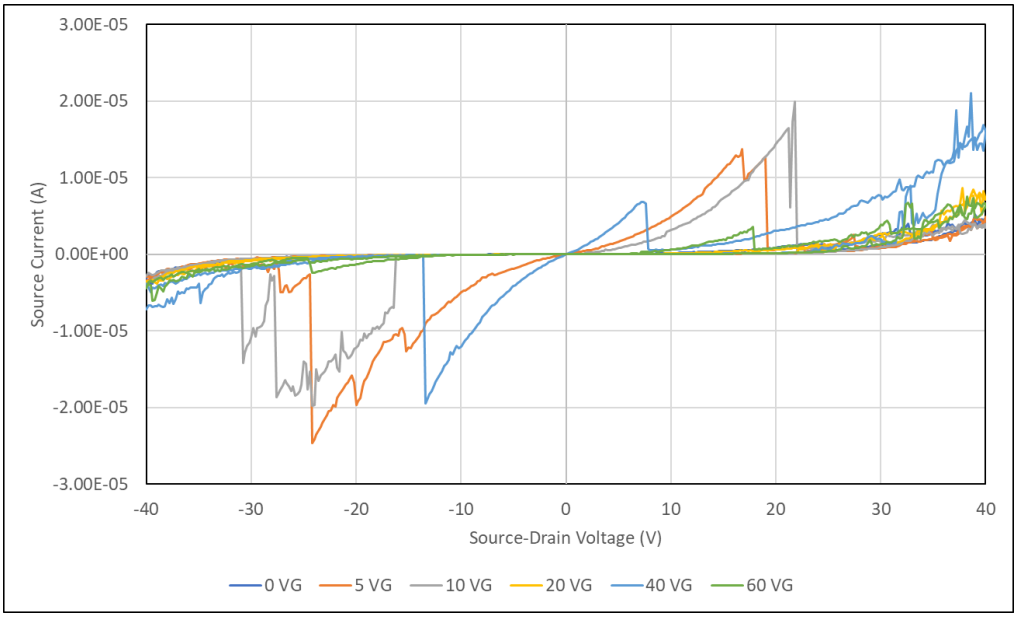
[Figure 46: 3D view of crystal surface, grown in trench.]

Electrical Characteristics



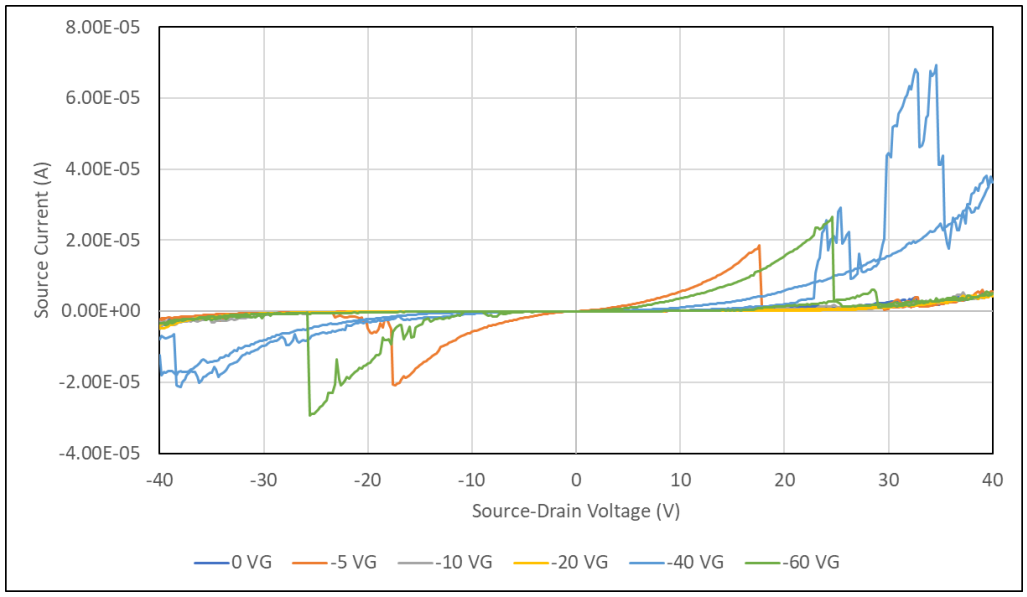
[Figure 47: Electrical characterization set up.]

Three probes were used on the Cronus 4-point probe station, one on the copper contact for the gate to apply a bias voltage, and two on the source and drain contacts, as shown in Figure 47 above, to measure current as the voltage was swept from -40 V to +40 V. Figure 48 below shows this sweep for a BC FET while applying the following gate bias voltages, 0 V, 5 V, 10 V, 20 V, 40 V, and 60 V.

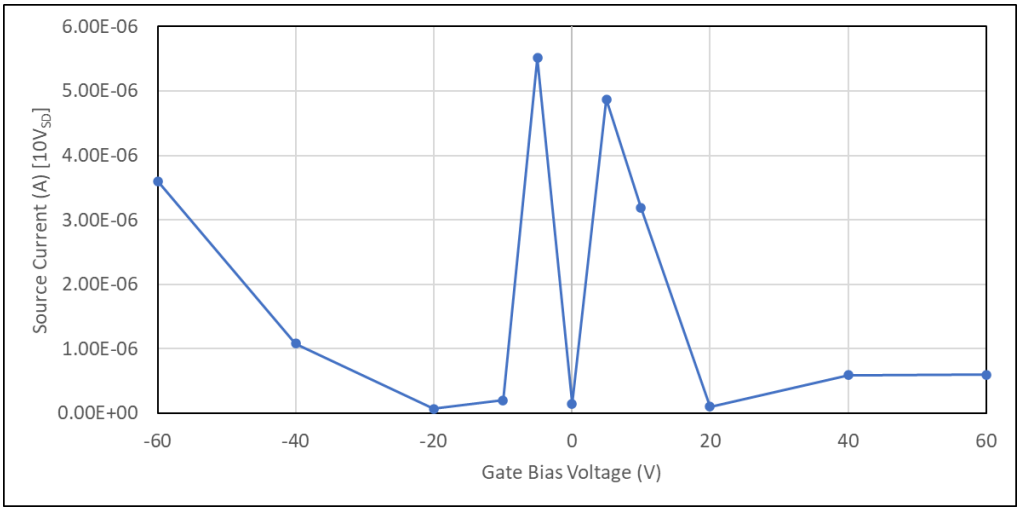


[Figure 48: Voltage sweep of $MAPBr_3$ perovskite BC FET.]

These measurements were also taken for the negative gate bias voltages as well, shown in Figure 49. Figure 50 shows a comparison of the positive and negative gate bias voltage sweeps at $V_{SD} = 10\ V$. The current dropped more at -10 V than it did for +10 V, and the current at -40 V and -60 V increased more than the +40 V and +60 V gate bias voltages. Overall, these results are qualitatively similar to the results recorded by Weili Yu et al. However, there is some strange behavior in the source current as the SD voltage is swept and the gate voltage increases.



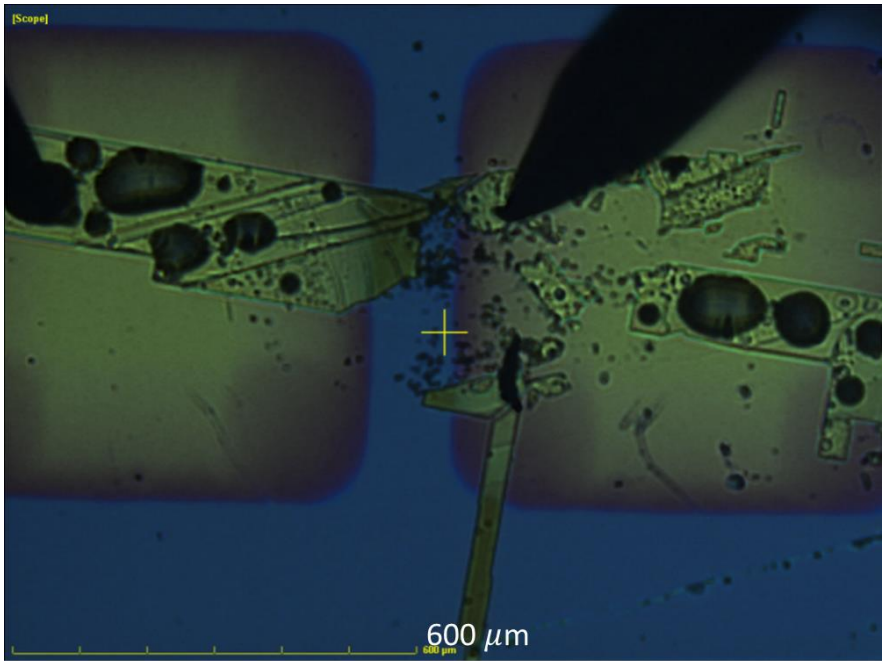
[Figure 49: SD voltage sweep for increasingly negative gate voltage]



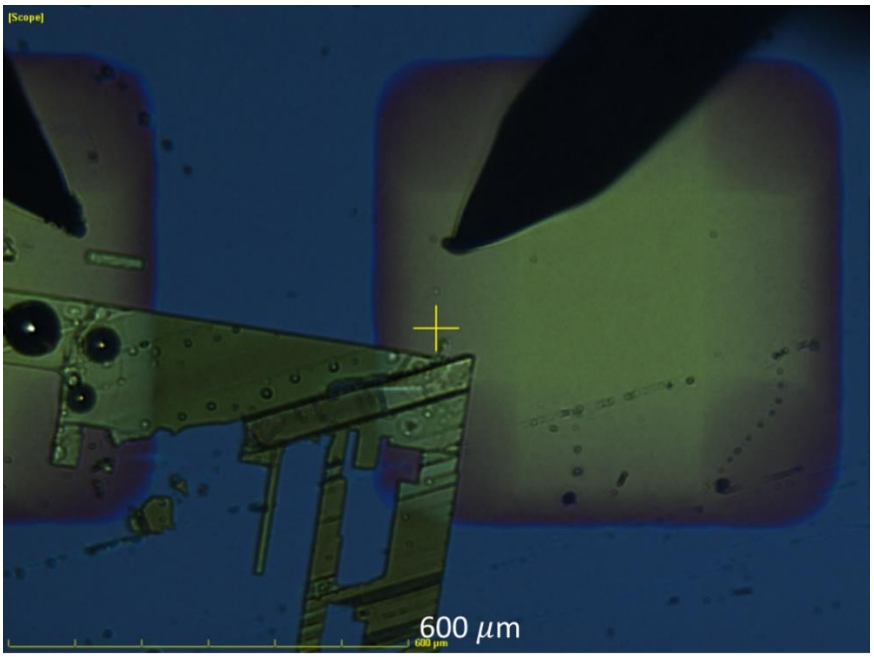
[Figure 50: Source current for gate bias voltage sweep at $V_{SD} = 10\ V$]

The TC devices had an issue of device connection, the crystal that connected two SD electrodes the correct channel length, 130 μm away from each other was broken as seen in Figure 51, possibly from the application or removal of the shadow mask. To avoid this channel length issue, the space between each contact would need to be made equal to the channel length. This will make it more likely to couple multiple electrodes together, but it will also make it more likely to have a functioning SD pair with the

desired channel length.



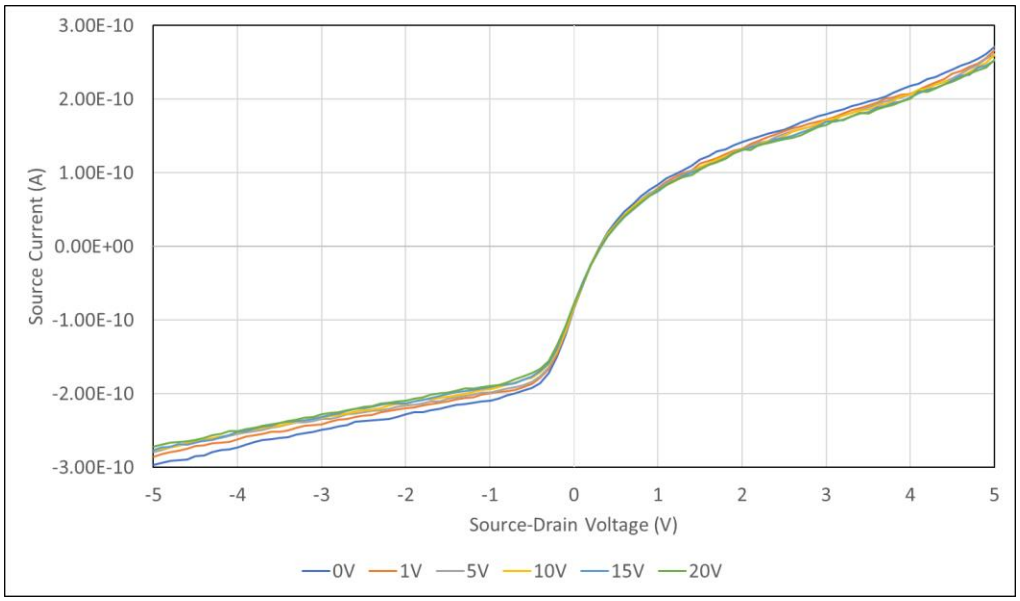
[Figure 51: Damaged perovskite single crystal channel.]



[Figure 52: Undamaged single crystal perovskite channel.]

Unfortunately, the other SD electrodes that were coupled with an undamaged

single crystal had the longer channel length, around 400 μm apart, as seen above in Figure 52. This longer channel length negatively affected the electrical characterization of the device. We see in Figure 53, that adjusting the bias voltage applied to the gate had little effect on the current, and the FET was unable to function properly, as seen by the non-Ohmic behavior of the graph. Additionally, the current is on the order of 20 – 30 nA, which is much lower than the current we saw with the BC device.



[Figure 53: Voltage sweep of $MAPBr_3$ perovskite TC FET.]

IV. CONCLUSIONS & RECOMMENDATIONS FOR FUTURE WORK

Using thin films to space the substrates during crystal growth such as PET or aluminum foil is prone to wrinkling resulting in inconsistent single crystal growth height. Using patterned silicon, we can space the substrates more accurately as well as direct the single crystal growth. Additionally, binder clips provide uneven pressure causing crystals to start forming in areas under the clip first and makes other crystals directly underneath the clip more likely to stick to the patterned substrate when separated from the BC, or the TC SiO_2 substrates.

Single crystal perovskite growth can be done using photolithography patterned silicon chips, but better control over the pressure applied during space confined growth is required to ensure the quality of the crystals grown. The use of a custom clamp improves the control but tuning the screws can leave one side or corner with less pressure than the other three, to solve this issue, springs could be implemented between the top of the M4 screws and the plexiglass using a washer, to help further ensure even pressure over the sample; in general crystals grown with less pressure had smaller crystals. This could also be helped by using a torque wrench to apply a specific force to the substrates, but the minimum force must be lower than 10 inch-pounds (in-lb) which is the minimum value of our torque wrench that cracked samples from over tightening. Additionally, the neoprene rubber balls may help distribute the pressure more equally, however they also seem to become more flexible when heated. To avoid this a heat resistant and rigid material would need to be cut to fit the clamp design and allow ink deposition while the substrates are in the clamp. The contact between the substrates should also be improved to avoid having crystals grow under the hills instead of in the trenches of the pattern. This

could be done by using thinner Si wafers such as 100 μm rather than 500 μm, or by including polydimethylsiloxane (PDMS) in the patterned substrate creation process before photolithography so that it remains at the top of the hills after patterning.

From our electrical characterization, we know the source drain contacts used in FET devices should be kept to the minimum size needed for electrical characterization, or risk current leakage. The reduced size of the contacts also improves the device reproducibility, because more source-drain pairs can be placed on the sample, increasing the chance of perovskite crystals growing across the channel in BC and TC devices. It is important to have equal spacing for TC electrodes, to increase the chance of a single crystal connecting the proper channel length.

V. SUMMARY

This thesis research topic revolved around single crystal perovskites grown using the space-confined growth technique developed by Weili Yu et al.[8] as a basis. Silicon wafers were patterned via photolithography coupled with ICP/RIE dry etching for the stripe patterned and TC substrates, or with chemical wet etching for the BC substrate. These wafers were broken into 1" x 1" chips and clamped together using small binder clips, 50 g and 100 g weights, and lastly a custom-made clamp, leaving an edge to inject the perovskite solution to be drawn in via capillary action. Once the $MAPbBr_3$ solution was drawn into the samples they were placed on a hotplate to anneal at 80°C for 48 hours. The single crystal growth from the various clamping methods was compared and we found that the crystal grown with binder clips were localized to areas near and directly under the clamp, and crystals directly underneath tended to stick to the patterned substrate. The use of weights distributes the pressure more evenly causing crystals to grow throughout the sample, but the pressure was insufficient to keep the solution in the striped pattern's trenches. Finally, the custom clamp distributes pressure more evenly than the binder clips and can provide enough to direct the perovskite single crystal growth. PTAA was included for a few samples in an attempt to increase the crystal size by increasing the substrate's surface hydrophobicity but was excluded from most samples to avoid affecting the electrical characterization.

Areas that need improvement include, the contact between the patterned and contact substrates, precise control over the pressure applied by all four bolts in the custom clamp, and the design of the source-drain electrodes. Extra space between the contacts can be caused by dust, or warped substrates, and can allow perovskite precursor

solution to leak and grow crystals in areas of the sample where we expected none. Using thinner Si wafers for substrate patterning and/or depositing PDMS before creating the patterned substrate can help improve this. If the bolts apply different pressures the crystal growth can be denser in some areas of the sample than others, and if altogether they do not apply enough pressure, the crystals grown are smaller on average. This can be counteracted with a torque screwdriver, to apply a specific force with each bolt. Lastly, the design of the SD electrodes should have contacts just large enough to land probes on for electrical characterization, and each contact should be the same distance away from the neighboring contact on all sides to increase the chance of creating a device.

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