Integration of broken-gap heterojunction InAs/GaSb Esaki tunnel diodes on silicon

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This study entails a comparison of the broken-gap InAs/GaSb heterojunction system on two different substrates, including Si and native GaSb as a control. Through the use of different integration schemes such as AlSb and $SrTiO_3$ buffer layers, GaSb was grown on miscut Si substrates using solid-source molecular beam epitaxy. The InAs/GaSb p^+-i-n^+ heterostructures were grown on the GaSb/Si virtual substrates and compared in terms of their surface morphology and crystalline quality. Esaki tunnel diodes were fabricated, and their performance compared across the different integration platforms. The control sample shows the best peak current density of 336 kA/cm^2 and a conductance slope of 274 mV/decade compared to the broken-gap junction on $SrTiO_3$/Si and AlSb/Si virtual substrates. These results show the possibility of integrating the InAs/GaSb system in ultralow power tunnel field-effect transistors logic applications with the cost-effectiveness and maturity of the silicon technology. © *2015 American Vacuum Society.*

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I. INTRODUCTION

Continuous scaling of traditional Si CMOS technology has been responsible for the advancement of the semiconductor industry in the past few decades. However, shrinking the devices comes at the cost of degraded electrical performance in logic applications by reducing the I_{on}/I_{off} ratio. Another inherent issue with device scaling is the power consumption, which can be improved by reducing the supply voltage (V_{DD}) for integrated circuits.[1] In recent years, there has been a drive to replace the traditional Si channel with III–V semiconductors that have lower effective masses and high carrier velocities and mobilities for ultralow power electronic applications.[2] Owing to the unavailability of larger wafer sizes for III–V substrates and the cost disadvantage for high-volume manufacturing, such implementation would require the monolithic integration of various III–V materials on silicon with low enough surface defects to fabricate surface channel transistors. The integration of III–V compound semiconductors with Si can also combine the cost advantage and maturity of the Si technology with the superior electrical and optical performance of these III–V materials. Along with a new integration platform, the tunnel field effect transistor (TFET) has emerged as a possible replacement for the traditional CMOS architecture.[3] The TFET operates using the principle of band-to-band tunneling where charged carriers are transferred from one energy band to another with a gated p^+-i-n^+ structure.[4] This allows a subthreshold swing (SS) of less than 60 mV/dec at 300 K, which is the fundamental limit in conventional MOSFETs due to thermal injection of charged carriers over a potential barrier.[4] Reducing the SS below the fundamental limit for traditional Si CMOS can enable ultralow power electronics with $V_{DD} < 0.5$ V. Therefore, the integration of III–V TFETs on a Si platform is highly desirable for next-generation post-CMOS microelectronics.

However, an inherent issue in TFETs is the realization of high ON currents (I_{on}), which is limited by the transmission probability of the interband-tunneling barrier. The broken-gap heterojunction consisting of n-InAs and p-GaSb, has been shown to have the lowest effective tunneling barriers and is one of the top candidates for high on current in III–V TFETs.[5] Record high I_{on} of 180 μA/μm at $V_{DS} = V_{GS} = 0.5$ V with an I_{on}/I_{off} ratio of 6×10^3 have been reported for gate-recessed vertical InAs/GaSb TFETs.[6] This broken-gap heterojunction has also shown the highest peak current density of 2.2 MA/cm^2 and Zener current density of 11 MA/cm^2 at -0.3 V as a result of optimized band-to-band carrier tunneling in heavily doped Esaki tunnel diodes.[7] All these results have been obtained through lattice-matched molecular beam epitaxy (MBE) grown on GaSb substrates. Conversely, while growing III–V semiconductors on lattice mismatched substrates, dislocations and structural defects can dominate the heterostructure and enhance Shockley–Read–Hall generation-recombination (G-R) as well as trap-assisted tunneling or interband tunneling increasing the OFF state current.[8] The crystalline and interface quality of the III–V heterojunction plays a significant role in determining higher I_{on}, lower I_{off}, and an improved I_{on}/I_{off} ratio.[9] Therefore, the integration of InAs/GaSb broken-gap heterojunction on

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lattice-mismatched substrates needs the careful selection and implementation of suitable MBE growth techniques that minimize the propagation of threading dislocations into the active device region.

In this work, we compare the structural properties, surface morphologies, and electrical performance of InAs/GaSb p^+-i-n^+ Esaki diodes with a GaSb i-layer on various platforms, viz., GaSb (control), $SrTiO_3$/Si, and AlSb/Si. Since TFETs operate as reversed-biased p^+-i-n^+ diodes with a gate over the intrinsic region, the OFF state current of a TFET can be defined as the reverse bias current or leakage current. Esaki diodes, which are degenerately doped versions of regular p-n junctions, are ideal candidates to study electrical characteristics of the base TFET structure. The forward bias characteristics for Esaki tunnel diodes include parameters such as peak current density (J_p), peak voltage (V_p), valley current density (J_v), and valley voltage (V_v), which are important criteria for evaluating the tunneling characteristics at the heterojunction. Conductance analysis is performed to relate the negative differential resistance (NDR) characteristics of the Esaki diodes to the TFET subthreshold swing for two-terminal devices and assess the tunneling probability, which depends directly on the peak current density. By comparing the performance of the same device structure on several different platforms, we can assess the advantages and limitations for various integration schemes. The results presented here hold important implications for the integration of III–V TFETs on Si substrates for future advancement of low-power electronic applications.

II. EXPERIMENT

All samples for this study were grown using MBE in a multichamber interconnected UHV system that allows for the growth of the oxide buffer layers in one chamber and transferring into the III–V growth without exposure to atmosphere, thus maintaining a clean well-ordered semiconductor surface. The solid source III–V chamber has a base pressure of $<5 \times 10^{-10}$ mbar pumped using a combination of ion, cryo, and titanium sublimation pumps. Growth rates were determined using the typical reflection high-energy electron diffraction (RHEED) oscillation technique, and the substrate temperature was measured using an optical pyrometer. The basic p^+-i-n^+ structure consisting of p^+ GaSb and n^+ InAs was grown on various substrates for comparison of crystalline quality, defects, and surface morphology along with electrical performance. For the control sample (TD1) as shown in Fig. 1(a), a 300 nm p^+ GaSb (Be-doped: $5 \times 10^{18}\,\text{cm}^{-3}$) was grown on a p-GaSb (001) substrate with a 0.35° miscut in the $\langle 111 \rangle$ direction, followed by a 3 nm thick intrinsic GaSb layer and a top layer of 25 nm n^+ InAs (Te-doped: $1 \times 10^{19}\,\text{cm}^{-3}$). The thickness of the InAs was so chosen as to not exceed the critical thickness, h_c, for this system according to the Matthews–Blakeslee model[10]

$$h_c = \frac{a_0\left(1 - \frac{\nu_{PR}}{4}\right)\left[\ln\left(\frac{h_c\sqrt{2}}{a_0}\right) + 1\right]}{2\sqrt{2}\pi|f|(1 + \nu_{PR})}, \qquad (1)$$

where a_o is the lattice constant of the substrate, f is the lattice mismatch between the substrate and the epilayer, and ν_{PR} is Poisson's ratio. For an InAs epilayer on GaSb substrate, the critical thickness is almost 40 nm before relaxation occurs, leading to misfit and threading dislocations in the epilayer.

For growth on the native GaSb substrates, the homoepitaxial growth of the GaSb buffer layer was carried out at a substrate temperature of 510 °C and a V/III flux ratio of 10. The integration of GaSb on Si (001) is quite challenging, as it involves not only a large lattice mismatch of 13% but also the growth of a polar material on a nonpolar substrate creating antiphase domains in the epilayer.[11] We employed two different buffer layer schemes to achieve high quality growth of GaSb on Si (001) substrates. The first approach involved the growth of an AlSb buffer layer on Si (001) using the interfacial misfit dislocation (IMF) array technique where highly two-dimensional periodic arrays of pure-edge 90° misfit dislocations can be formed in both the [110] and [$\bar{1}$10] directions, relieving most of the excess strain due to the 12% lattice mismatch at the AlSb/Si heterointerface.[12] The periodic nature of the misfit dislocations is evident from the fact that exactly eight AlSb lattice sites can be grown on nine Si lattice sites along the [110] direction.[13] Since 90° pure-edge dislocations

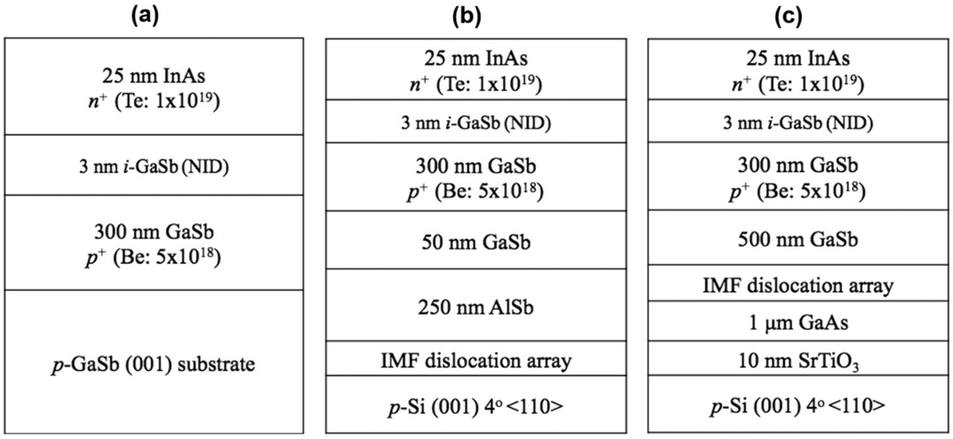

FIG. 1. InAs/GaSb broken-gap p^+-i-n^+ Esaki tunnel diode structures grown using MBE on (a) native GaSb substrate—TD1, (b) miscut Si substrate using an AlSb buffer layer—TD2, and (b) using an $SrTiO_3$/GaAs buffer scheme—TD3.

travel parallel to the growth plane rather than into the epilayers, the structural quality of the GaSb epilayer grown on Si is close to the optimal under this technique. The IMF growth process involved exposing a clean Si surface to a flux of Sb followed by the deposition of 3–4 monolayers of Al 500. Following this, a 250 nm thick AlSb buffer layer was grown before the growth of the GaSb layer and the *p-i-n* heterostructure. The use of miscut substrates, in this case, a Si (001) miscut 4° toward the $\langle 110 \rangle$ direction, also aids in the suppression of antiphase domain (APD) boundaries by utilizing the double-atomic step-edge, leading to APD annihilation. The AlSb layer now serves as a buffer layer for the subsequent growth of GaSb, which is more closely lattice-matched to AlSb than Si. The p^+-i-n^+ structure is then grown on top of the 50 nm GaSb layer, and the complete structure (TD2) grown using this approach is shown in Fig. 1(b).

The second buffer layer scheme involves the growth of a crystalline oxide buffer layer of $SrTiO_3$ (STO) on a Si (001) miscut substrate to integrate high-crystalline quality GaAs. The $SrTiO_3$ lattice ($a_{STO} = 3.905$ Å) undergoes a 45° rotation to accommodate the high lattice mismatch with the underlying Si (001) ($a_{Si} = 5.431$ Å), leading to a strain of 1.7%.[14] The GaAs lattice ($a_{GaAs} = 5.653$ Å) grown is now strained 2.3% with respect to the 45° rotated $SrTiO_3$ lattice, thereby enabling the reduction from the original 4% strain for the GaAs/Si system.[15] The growth of the STO layer on Si is described in detail in Ref. 14. Briefly, the oxide layer was deposited on a Si substrate in a separate interconnected MBE chamber using elemental sources and molecular oxygen. The initial nucleation of the oxide layer growth was carried out at 300 °C followed by a high temperature (550 °C) growth for the bulk of the film at an oxygen pressure of $\sim 5 \times 10^{-6}$ mbar. The growth of GaAs on the STO oxide layer was achieved using a two-step growth process in which a GaAs nucleation layer of 25 nm was grown at a temperature of 450 °C using an As_2/Ga ratio of 8 and a growth rate of 0.15 ML/s. Following this, the growth temperature was decreased to 380 °C and 1 μm of GaAs was deposited at an As_2/Ga ratio of 15 and growth rate of 0.5 ML/s. Finally, a postgrowth anneal was carried out at 580 °C for 15 min with the entire growth process monitored using *in situ* RHEED. Recent work has shown that a Sr-terminated STO surface has the optimum surface energy for successful wetting of GaAs epilayer and results in GaAs films with improved structural qualities and extremely smooth surface morphologies.[16] The successful growth of STO buffer along with GaAs epilayer is followed by the IMF growth of 500 nm GaSb layer as discussed above. Following this, the same InAs/GaSb p^+-i-n^+ Esaki diode structure is grown as for all the other samples. The complete structure (TD3) grown using the STO buffer scheme is shown in Fig. 1(c). The structural properties of all the grown samples were characterized using double crystal x-ray diffraction (XRD) and the surface morphologies were mapped using atomic force microscopy (AFM) in tapping mode.

Esaki diode fabrication was performed using general procedures established in prior work.[17] First, the sample surface was cleaned in a 10:1 H_2O:HCl solution for 10 s, followed by a 200 nm thick layer of molybdenum (Mo) using RF sputtering. Negative resist, nLOF, diluted in Propylene glycol monomethyl ether acetate (PGMEA) (≈1:1) and e-beam lithography defined the metal contacts. SF_6-based reactive ion etching was used to define mesa contacts ranging from 100 nm to 20 μm^2. A brief oxygen surface clean was used to remove residual photoresist. A 20:1 citric acid ($C_6H_8O_7$): hydrogen peroxide (H_2O_2) solution etched the sample for 65 s to form Esaki diode mesas. The contact area and undercut were measured for representative devices in a scanning electron microscope to increase the precision of the J_P estimation. Bis-benzocyclobutane was then used as an interlayer dielectric (ILD) and planarization layer as detailed by Pawlik *et al.*[7] Level 2 metal contacts were then defined by a second e-beam lithography and a lift-off process, producing devices depicted in Fig. 2. The electrical properties of the InAs/GaSb tunnel diodes were assessed by measuring the current–voltage (*I-V*) characteristics using a Keithley 4200 Semiconductor Parameter Analyzer. A large area Esaki diode (greater than 1000× the measured junction area) was used as a virtual ground. The ground plane was designed to fully surround the devices to minimize any effect from current crowding as this is critical for measuring high current density tunnel junctions and minimizes unwanted resistive latching that obscures the NDR. Data were collected for over 100 devices on each of the three different platforms including the control sample, $SrTiO_3$ buffer on Si, and AlSb buffer on Si. J_P and J_V were extracted and corrected based on the area analysis and a statistical analysis was performed to get a representative value of J_P and conductance slope for the broken-gap Esaki tunnel diodes on silicon using different buffer layer schemes.

III. RESULTS AND DISCUSSION

A. Structural properties and surface morphology

To assess the crystalline quality and strain properties of the epilayers grown for the three different samples, high-resolution x-ray diffraction measurements were carried out on a Bede-D1 diffractometer with a Cu-K$_{\alpha 1}$ x-ray source. Figure 3 shows the high resolution omega-2theta scans for the GaSb (004) and InAs (004) diffraction peaks in the p^+-i-n^+ structure for the three samples. These spectra show the presence of strained InAs with respect to the underlying

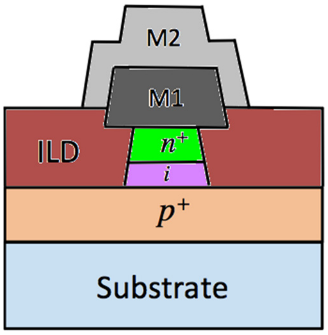

FIG. 2. (Color online) Schematic showing the cross section of the Esaki diode processed for electrical characterization. The second level metal and ILD must be used with these mesas to contact devices below 2 μm widths.

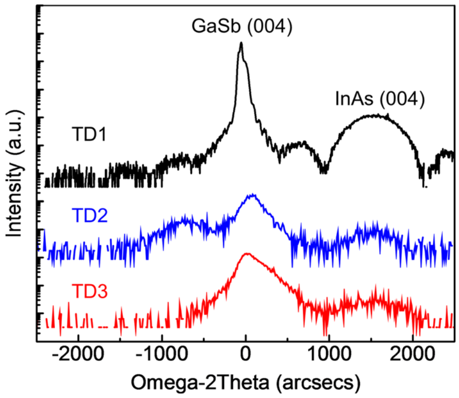

FIG. 3. (Color online) High resolution omega-2theta scan showing the GaSb (004) and InAs (004) diffraction peaks for the samples used in this study. The InAs epilayer is grown below the critical thickness to avoid relaxation and is pseudomorphically strained with respect to the underlying GaSb lattice for all the samples.

GaSb lattice as expected since the InAs layer is grown below its critical thickness to avoid strain relaxation that can lead to defects in this epilayer. An important metric to compare across the different integration platforms is the threading dislocation density in the GaSb epilayer, which is directly influenced by the epitaxial quality of the underlying buffer layers and substrates. Therefore, to determine the crystalline quality of the GaSb epilayers, rocking curve analyses, i.e., omega scans, were performed for the GaSb (004) diffraction peak, which can estimate the threading dislocation density (TDD) from the full-width at half-maximum (FWHM).[18] Equation (2) can be used to estimate the TDD using the FWHM of the GaSb (004) rocking curve

$$TDD \approx \frac{\beta_m^2}{4.36\, b^2}, \tag{2}$$

where β_m is the FWHM in units of radians and b is the Burgers vector, which is assumed to be $a/2[110]$ for GaSb. The defect densities obtained are only an approximation since the GaSb thicknesses are not the same for the three samples which directly influences the FWHM. Surface morphology is also an important parameter for device fabrication as a smooth surface leads to ease in defining device patterns as well as aids in careful etching of the device layers. Surface features also give an insight into the crystal defects within the epilayers of the grown structure. A Veeco Dimension-3100 AFM with a Si tip in tapping-mode was used to compare the surface features and the root mean square (RMS) roughness among the different samples.

TABLE I. Comparison of the TDD and the RMS surface roughness of all three samples.

Sample	FWHM (arc sec)	TDD (cm^{-2})	RMS (nm)
TD1	50	Lattice-matched	0.11
TD2	1408	5.77×10^9	5.74
TD3	883	2.27×10^9	2.32

Table I shows a comparison of the dislocation densities and RMS surface roughness in the GaSb epilayer across the different integration platforms. The control sample TD1 shows the lowest value of FWHM since it employs a lattice-matched epitaxial growth mode. The RMS surface roughness of 0.11 nm is indicative of the Frank–van der Merwe growth mode where the incoming adatoms attach preferentially to surface sites, resulting in atomically smooth surfaces. The atomic step edges are evident in the surface morphology, which shows that the substrate surface topography was clearly transferred throughout the growth of the whole structure to all the epilayers since the GaSb (001) substrate used was miscut 0.35° in the ⟨111⟩ direction [Fig. 4(a)]. Homoepitaxy of GaSb is usually plagued with oval surface defects as a result of limited adatom diffusion on the surface, but no such defects were observed in sample TD1 as the growth proceeded in the step-flow regime producing an extremely smooth surface.[19]

The p^+-i-n^+ structure grown on miscut silicon using the AlSb buffer layer approach, TD2, shows a much larger value of the rocking curve FWHM, which can be attributed to the dislocations originating at the AlSb-Si heterointerface. The IMF growth of AlSb on lattice-mismatched Si surface produces a significant number of 60° misfit dislocations along with the nonpropagating 90° pure-edge dislocations.[20] Ideally, if the growth technique produces only 90° dislocations, then no threading segments are produced since these dislocations are elastically stable and cannot glide in the closed packed {111} planes. However, there is always a finite number of 60° dislocations that nucleate in the AlSb epilayer and can easily glide along the {111} planes resulting in threading segments. This sample also exhibits a high RMS surface roughness of 5.74 nm, and there are no spiral features observed in this case except for the presence of mounds over the entire surface [Fig. 4(b)]. Group III adatoms that arrive on the surface during the

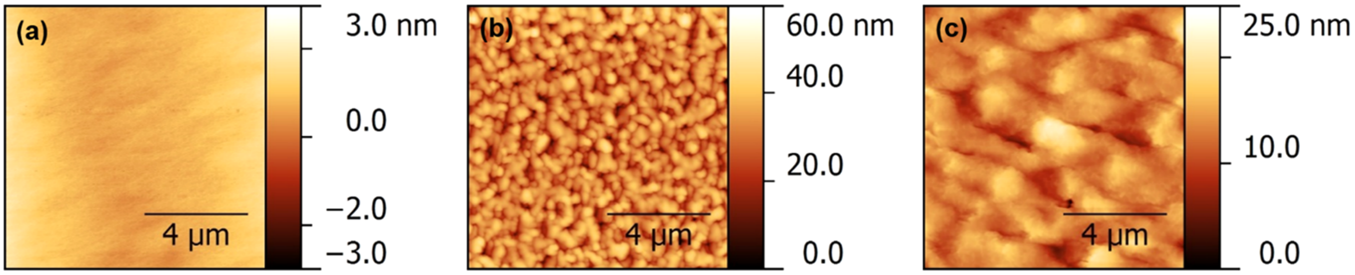

FIG. 4. (Color online) AFM micrographs of 10 × 10 μm areas for (a) control sample—TD1 (b) InAs/GaSb p^+-i-n^+ on AlSb/Si—TD2. (c) Esaki diode on GaAs/STO/Si—TD3.

growth process with a high density of screw dislocations preferentially attach themselves on the step-edge of these spiral features, and as growth proceeds, the different spiral mounds coalesce, leading to a steady-state step-flow growth mode. Although the screw dislocations created at the AlSb–Si interface propagate through the epilayers, the shorter diffusion length of the Al adatom is responsible for the absence of spiral features, which is commonly observed for the growth of GaSb on lattice-mismatched substrates.[21] Another reason that leads to the broadening of the rocking curve is the large thermal mismatch between the III–V layers and the Si substrate. During the cool down period from growth temperatures of around 500 °C to room temperature, the component layers contract at different rates, creating additional structural defects within the p^+-i-n^+ stack.

For sample TD3 grown using the GaAs/STO buffer on Si, the dislocation density is less than half compared to TD2, and the RMS surface roughness is also reduced to 2.32 nm. Although the same type of 60° and 90° dislocations and structural defects are present here as in the samples above, the reduction in dislocation density is due to the fact that this integration technique creates lower number of defects as the lattice mismatch is gradually reduced over the intermediate STO buffer layer. The resultant GaAs layer is much smoother and has a lower dislocation density as compared to GaAs grown directly on Si. This provides a smoother and higher crystalline quality platform for the IMF-based growth of GaSb on the GaAs epilayer. The surface morphology shows some evidence of spiral features as the Ga adatom diffusion length is large enough to have sufficient mobility on the surface during growth [Fig. 4(c)].

B. Electrical properties

The working principle of the InAs/GaSb broken-gap Esaki tunnel diodes can be easily understood in terms of the energy band diagram. A one-dimensional Poisson solver was used to calculate the conduction and valence band profiles for the InAs/GaSb junction at equilibrium as well as under forward and reverse bias. At a zero applied bias, the effective tunneling barrier, which corresponds to the difference between the conduction band in InAs and the valence band of GaSb at the interface, is −150 meV [Fig. 5(a)]. As forward bias is applied, increased band-bending leads to the lowest conduction subband on the InAs side to be pushed above the highest hole subband on the GaSb side, disabling direct band-to-band tunneling. This leads to the observation of a NDR region in the I-V characteristics [Fig. 5(b)]. In case of reverse bias [Fig. 5(c)], electrons in the valence band of the p^+ side tunnel directly toward the empty states present in the conduction band of the n^+ side creating large tunneling current, which increases with the application of reverse voltage.

To evaluate the InAs/GaSb tunnel junction, Esaki diodes were fabricated on all three samples using a well-established technique as detailed in the previous section. The electrical properties were assessed by measuring the current–voltage (I-V) characteristics using a Keithley 4200 Semiconductor Parameter Analyzer. Since a TFET is just a gated p^+-i-n^+ diode, two-terminal Esaki diode measurements offer a great alternative to separate the parasitic effects of the third-gate oxide terminal and assess solely the quality of the tunneling junction and the heterointerface. Using two-terminal measurements, the electrical characteristics of the Esaki p^+-i-n^+ junction can be used to study the effect of structural defects and interface quality on device performance. The absolute conductance (G) of the junction in the NDR region can be used to examine the scenario in a diode, and the conductance slope (G^*) gives a comparable metric to the subthreshold slope for a TFET, if the diode was converted to a three-terminal device.[22] The peak current density (J_p) in the forward bias mode is directly related to the band-to-band tunneling mechanism and is indicative of the ON current in a TFET. More than 100 devices were measured for each sample with areas ranging from 500 × 500 nm to 1 × 1 μm, and representative values of peak current density and conductance slope were extracted for all samples by doing a statistical analysis and using a Gaussian fit to achieve the mean value and standard deviation. Figure 6(a) shows the representative J-V and G-V curves for control sample TD1 for a device with a cross-sectional area of 1 × 1 μm. It is also important to note that the conductance slope is calculated in the NDR region of the Esaki-diode G-V curve. Even though there are some instability-driven oscillations in NDR region, an average value of the conductance slope can be calculated in this region using the following equation:

$$G^* = \frac{|V_p - V_v|}{\left|\log_{10}\left(\frac{J_p}{V_p}\right) - \log_{10}\left(\frac{J_v}{V_v}\right)\right|} \text{ mV/decade}, \tag{3}$$

where all the parameters have been defined previously. The statistical distributions for the extracted J_p and G^* are shown

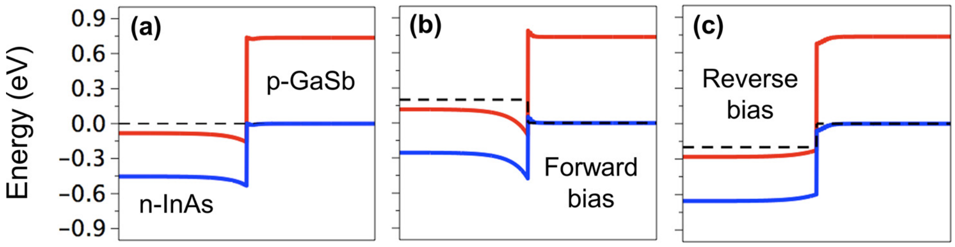

Fig. 5. (Color online) Poisson simulations for the band diagram calculation of the InAs/GaSb p^+-i-n^+ diode at (a) equilibrium (b) forward bias at +0.20 V and (c) reverse bias at −0.20 V.

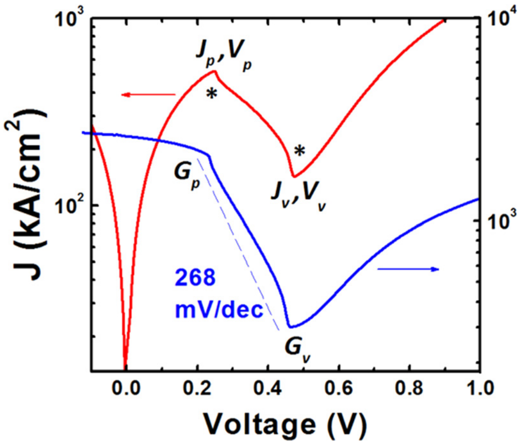

FIG. 6. (Color online) Representative *I-V* and corresponding *G-V* curve shown along with the extraction of conductance slope in the NDR region for sample TD1.

in Figs. 7(a) and 7(b), respectively. Control sample TD1 shows the highest value of $J_p = 336 \pm 79\,\text{kA/cm}^2$ and $G^* = 274 \pm 22\,\text{mV/decade}$. TD2 shows a much lower J_p of $119 \pm 31\,\text{kA/cm}^2$ and $G^* = 381 \pm 85\,\text{mV/decade}$, which can be attributed to the increased number of structural defects in this sample as seen from the XRD and AFM analysis. The presence of defect states in the band-gap at the InAs/GaSb interface can lead to leakage in the OFF state due to trap-assisted tunneling. This phenomenon tends to increase the valley current in the NDR region and hence increases G^*. Additionally, the change in band alignment at the interface due to the presence of these electrically active defects can cause local band-bending and blurring of the turn-off mechanism, leading to a less steep conductance slope and, therefore, much higher values of SS in TFETs.[23]

Sample TD3 with the STO/GaAs buffer layer scheme showed a J_p of $218 \pm 39.5\,\text{kA/cm}^2$ and $G^* = 304 \pm 44\,\text{mV/decade}$. The use of the STO/GaAs buffer on miscut Si substrates to integrate the broken-gap junction showed much improved performance and steepness of the conductance slope in comparison to sample TD2, which is attributed to the reduced dislocation density and structural defects observed in TD3. These results show the benefits of using the STO/GaAs buffer layer scheme to create high-quality III–V tunneling devices on a Si substrate. The large differences in J_p among all samples can be attributed to factors such as difference in doping levels as well as the abruptness of the doping at the heterojunction. According to Kane's model, the interband tunneling is directly proportional to the electric-field that exists at the InAs/GaSb interface, and the tunneling current is dependent on the strength of this field, which is controlled by doping profiles.[24] Additional SIMS analysis needs to be carried out to ascertain the doping profiles for all the different samples, which will provide more insight into the variations in J_p.

Integration of III–V devices on silicon presents a number of challenges not the least of which is the degradation of performance due to the high defect density of the III–V semiconductors when grown on silicon. While the results suggest pathways to integrate p^+-i-n^+ tunnel diode devices on silicon, buffer layers used to transition from the group IV to the III–V lattice constants need to be improved. The results obtained from this study suggest that the surface energy of the oxide buffer layer can be modified to allow for two dimensional growth of compound semiconductors. Improvement to the device performance is also possible if the tunnel devices are integrated onto small areas on the silicon substrates. Such concepts are currently being studied through selective area growth of the III–V materials on patterned Si substrates, and further studies are needed to explore this concept. A second advantage of using crystalline oxide layers on silicon is that they can be utilized as part of highly integrated functional devices, whereby the oxide layer can function as a ferroelectric and/or ferromagnetic material finding use in memory or sensor applications.

IV. SUMMARY AND CONCLUSIONS

In conclusion, broken-gap InAs/GaSb Esaki p^+-i-n^+ structures were grown using MBE on different substrates, viz., GaSb, AlSb/Si, and GaAs/STO/Si. The crystalline properties were determined using rocking curve XRD analysis, and the surface morphologies were measured using AFM. The III–V heterostructures grown on lattice-mismatched Si substrates showed the presence of increased threading

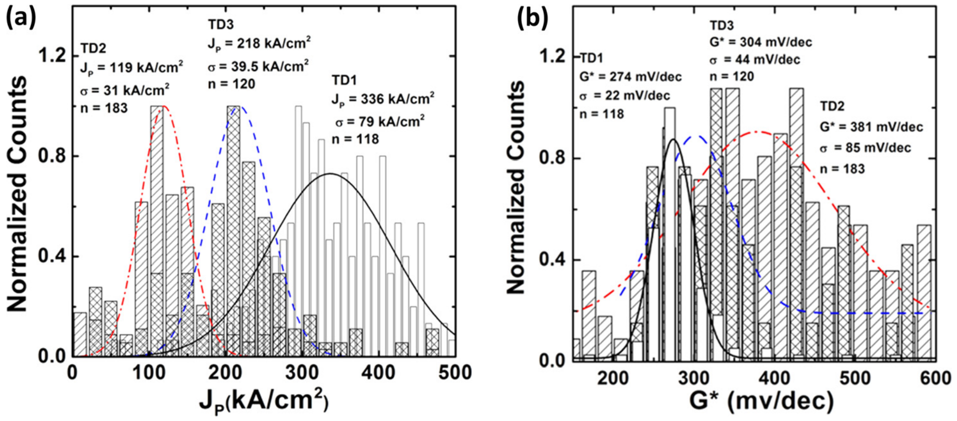

FIG. 7. (Color online) (a) Statistical distribution of the peak current densities for all samples and (b) statistical distribution of the conductance slope values for all samples.

dislocation density as compared to the control sample on the GaSb substrate. Esaki tunnel diodes were fabricated and characterized using *I-V* measurements and their performance was compared across the various substrates using the peak current density and conductance slope. Broken-gap devices on Si show less-steep conductance slope and lower tunnel current density, showing the need for improved buffer layers to produce GaSb with low structural defects on Si and achieve the same level of performance as lattice-matched substrates.

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