Journal of Applied Physics

Bias temperature stress induced hydrogen depassivation from Al_2O_3/InGaAs interface defects

Cite as: J. Appl. Phys. **123**, 025708 (2018); https://doi.org/10.1063/1.4994393
Submitted: 05 July 2017 . Accepted: 22 December 2017 . Published Online: 12 January 2018

Kechao Tang, Ravi Droopad, and Paul C. McIntyre

Bias temperature stress induced hydrogen depassivation from Al_2O_3/InGaAs interface defects

Kechao Tang,[1] Ravi Droopad,[2] and Paul C. McIntyre[1]
[1]*Department of Materials Science and Engineering, Stanford University, Stanford, California 94305, USA*
[2]*Ingram School of Engineering, Texas State University, San Marcos, Texas 78666, USA*

(Received 5 July 2017; accepted 22 December 2017; published online 12 January 2018)

We study the reliability of Al_2O_3/InGaAs metal-oxide-semiconductor gate stacks by investigating the effect of bias temperature stress on the charge trap density at the Al_2O_3/InGaAs interface and in the bulk oxide. Under extended negative biasing at 100 °C, the gate stacks display a notable increase in the interface trap density (D_{it}), but little change in the border trap density. This phenomenon is more prominent for samples exposed to a H_2/N_2 forming gas anneal (FGA) than for the as-deposited samples. Negative gate bias applied during 100 °C thermal stress negates the FGA-induced passivation of interface states and causes convergence of the D_{it} of the post-FGA and as-deposited gate stacks with increasing biasing time. This appears to be caused by hydrogen depassivation of interface traps under bias temperature stress, which is further supported by an observed hydrogen isotope effect when comparing the rate of D_{it} increase after annealing in hydrogenated versus deuterated forming gas. A N_2 anneal control experiment also indicates that the stability of the interface trap density of post-FGA Al_2O_3/InGaAs gate stacks is more strongly influenced by the behavior of hydrogen at the interface than by the thermal treatment effect of the anneal. *Published by AIP Publishing*. https://doi.org/10.1063/1.4994393

I. INTRODUCTION

For beyond-silicon complementary metal oxide semiconductor (CMOS) devices, $In_{0.53}Ga_{0.47}As$ is an attractive candidate for n-type channel materials due to its high electron mobility.[1,2] Atomic layer deposited (ALD) Al_2O_3 has high thermal stability and a large conduction band offset with respect to InGaAs,[3,4] prompting interest in it either as a dielectric layer for InGaAs field effect transistors,[5,6] or as a high band-offset interlayer between the InGaAs channel and other high-k dielectrics.[7] Due to the lack of a good native or thermally grown oxide, extensive research on InGaAs MOS devices has focused on the removal of charge traps, including those at deposited oxide/III-V interfaces,[8–11] and of border traps in the dielectric layer.[12–14] Much progress has been made in defect passivation and performance optimization over the past decade, leading to the development of high performance InGaAs MOSFETs with low interface defect density, excellent thermal stability, and high drain current of 1.84 mA/μm.[15–17] However, the bias temperature instability (BTI) of high-k/InGaAs MOS devices has taken on growing importance.[18–21] Degradation of InGaAs n-MOSFETs induced by bias temperature stress (BTS) has been reported routinely, affecting a number of device properties including the threshold voltage, the transconductance, the subthreshold swing, and the on-state current.[22,23] The BTS effect is much more pronounced than typical Si MOS devices and becomes a critical concern for the practical implementation of InGaAs-based CMOS.[24]

Despite several reports of BTI of high-k/InGaAs MOS, the underlying mechanisms are still not clearly understood. In separate publications, BTS-induced device degradation is ascribed to slow charge trapping in the gate oxide[24,25] or to the generation of charge traps at the oxide-InGaAs interface.[26,27] Pre-existing border traps in the high-k dielectric layer are also assumed to contribute to the transient instability of electrical characteristics of III-V based devices.[28,29] In addition, the extent of BTI instability of high-k/InGaAs gate stacks is affected by differences in device fabrication and the abruptness of the dielectric/semiconductor interface,[30,31] which complicates the understanding of BTS induced degradation. Finally, even though a number of these prior works electrically characterized traps generated or depassivated during BTS in InGaAs MOS devices, the atomistic origins of these defects remain elusive.

In this work, we systematically investigated the effect of BTS on the Al_2O_3/InGaAs gate stacks fabricated by an optimized *in situ* As_2 desorption recipe, which has previously been found to generate an abrupt and well-defined oxide/semiconductor interface.[31] Capacitance-voltage (C-V) data for Al_2O_3/InGaAs MOS capacitors after different durations of BTS were measured, and the evolution of both the interface trap density (D_{it}) and the border trap density (N_{bt}) was examined quantitatively. We also engineered Al_2O_3/InGaAs gate stacks with various post-ALD treatments, and the impact of BTS on these samples was carefully compared to gain a deeper insight into its physical mechanism.

II. MATERIALS AND METHODS

An n-type Si doped (1×10^{17} cm^{-3}) InGaAs (100) epilayer was grown lattice matched on InP substrates by molecular beam epitaxy (MBE). During the post-growth cooling of the MBE process, InGaAs was coated with an As_2 capping layer of ~200 nm thickness, which protects the InGaAs surface from oxidation and contamination during air exposure before loading into the ALD chamber. Immediately following the thermal desorption of As_2 capping at 350 °C in the

high vacuum ALD chamber ($\sim 10^{-6}$ Torr), ~4.5 nm of Al_2O_3 was deposited using 60 cycles of alternating trimethylaluminum (TMA) and H_2O pulses at a substrate temperature of 270 °C. The estimated doses per cycle was 900 L and 1200 L for TMA and H_2O, respectively, and the chamber pressure was maintained at 0.68 Torr by a continuous flow of dry N_2. After the ALD process, 30 nm thick circular (50–125 μm radius) Pd top electrodes and 100 nm thick Al back contacts were deposited by thermal evaporation.[32] Further details of the experimental methods can be found in Ref. 32. A subset of $Pd/Al_2O_3/InGaAs$ gate stacks was then annealed in $5\%H_2/95\%N_2$ forming gas at 400 °C for 30 min.

The electrical properties of the pristine gate stacks were characterized by multifrequency C-V curves from 1 kHz to 1 MHz at room temperature in the dark, using a HP4284A LCR meter. The trap density is quantitatively analyzed by a full interface state model[33] and a border trap model[34] through the fitting of C-V and conductance-voltage (G-V) data. The flatband voltage point (V_{fb}) was extracted by fitting the ideal C-V with the 1 MHz data,[35] which produced results consistent with the commonly used inflection point method.[36] BTS was performed by heating the samples to 100 °C, and then applying a steady positive or negative bias on the top Pd electrode for an extended duration (~30–60 min). The semiconductor chips were kept in a vibration-resistant probe station under lab air and in the dark during the BTS treatment. The samples were then cooled down to room temperature and C-V curves were measured with the same setup as that used prior to BTS. A schematic illustration of the measurement setup is shown in Fig. 1(a). The impact of BTS on the gate stacks was investigated by comparing the electrical measurement results before and after stressing.

III. RESULTS AND DISCUSSION

Figure 1(b) shows the C-V data for $Pd/Al_2O_3/InGaAs$ gate stacks after forming gas anneal (FGA) and before the BTS test. The extracted V_{fb} is ~0.7 V for the pristine devices before BTS. In the subsequent positive and negative BTS at 100 °C, the stressing voltages were set to 3.3 V and −2.0 V, respectively, to maintain similar voltage differences with respect to V_{fb} and comparable electric fields across the dielectric. The magnitude of the oxide electric field, taking into account the effect of the interface and border traps, is ~4.4 MV/cm for all cases in this study. C-V data were measured at room temperature after either positive or negative BTS at 100 °C for 30 min, as shown in Figs. 1(c) and 1(d), respectively. Compared to the pristine devices, a notable increase of the frequency response in inversion is detected after the BTS test, and this effect is especially significant after negative BTS testing [Fig. 1(d)]. This result indicates a BTS induced degradation of the $Al_2O_3/InGaAs$ interface with increased interface trap density (D_{it}), which is quantitatively confirmed by the full interface state model, as displayed in Fig. 1(e). The C-V data after the BTS test remain invariant during storage of the samples in lab air and in the light for weeks, indicating irrecoverable degradation of the interface of the MOS gate stacks. On the other hand, the border trap density (N_{bt}) is unaffected by the BTS test, showing a constant value of $9.0 \times 10^{19}\,cm^{-3}eV^{-1}$ at $E - E_C = 0.4$ eV for all samples. The positive BTS test also induces a slight positive shift of V_{fb}, which could be due to the generation of positive charge traps at the interface or in the bulk oxide. The lower accumulation capacitance in the samples after negative BTS is caused by a significant increase of D_{it} around the flatband region, which induces a Fermi level pinning effect. The greater negative bias temperature instability (NBTI) compared to positive bias temperature instability (PBTI) for high-k/InGaAs is consistent with a previous report.[37] Samples not subjected to bias show little change in C-V data after the heating process, indicating that the increase in D_{it} observed in Fig. 1 is not solely caused by 100 °C exposure to lab-air.

To investigate the cause of this BTS induced interface degradation, we performed similar BTS testing on $Al_2O_3/InGaAs$ gate stacks fabricated with an identical procedure, but without the post-metal FGA treatment. Due to the difference in V_{fb} compared to post-FGA samples, the negative BTS for these samples was set to −1.5 V to maintain a comparable electric field in the dielectric. The C-V data for the pre-FGA and post-FGA samples before and after the negative BTS test are shown in Figs. 2(a)–2(f). An increase of the inversion frequency dispersion with BTS time is observed for the pre-FGA gate stacks [Figs. 2(a)–2(c)], but the magnitude of increase is

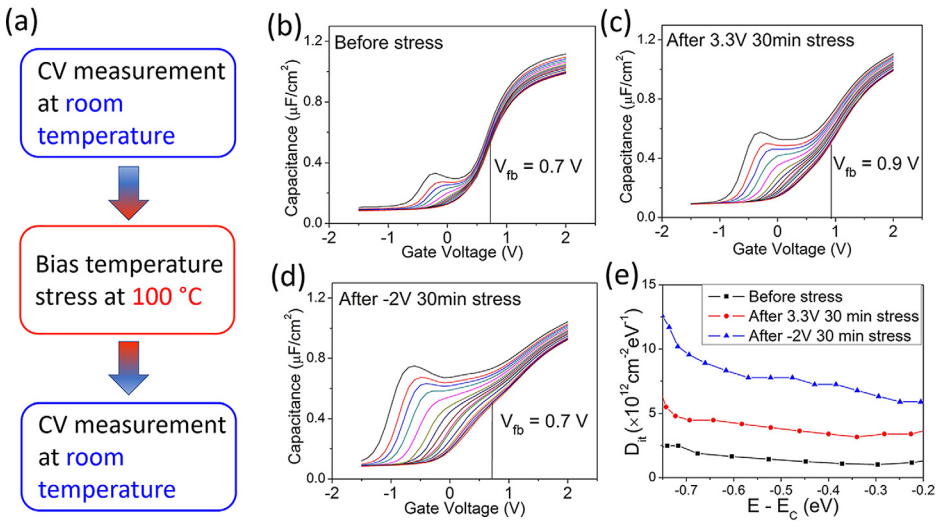

FIG. 1. Bias temperature stress for post-FGA $Al_2O_3/InGaAs$ gate stacks. (a) Procedure for bias temperature stress treatment and electrical characterization. (b)–(d) Multifrequency C-V measurements for post-FGA $Al_2O_3/InGaAs$ gate stacks before bias temperature stressing (a), after 3.3 V biasing at 100 °C for 30 min (b), and after −2 V biasing at 100 °C for 30 min (d). (e) Extracted D_{it} for all the samples in (b)–(d).

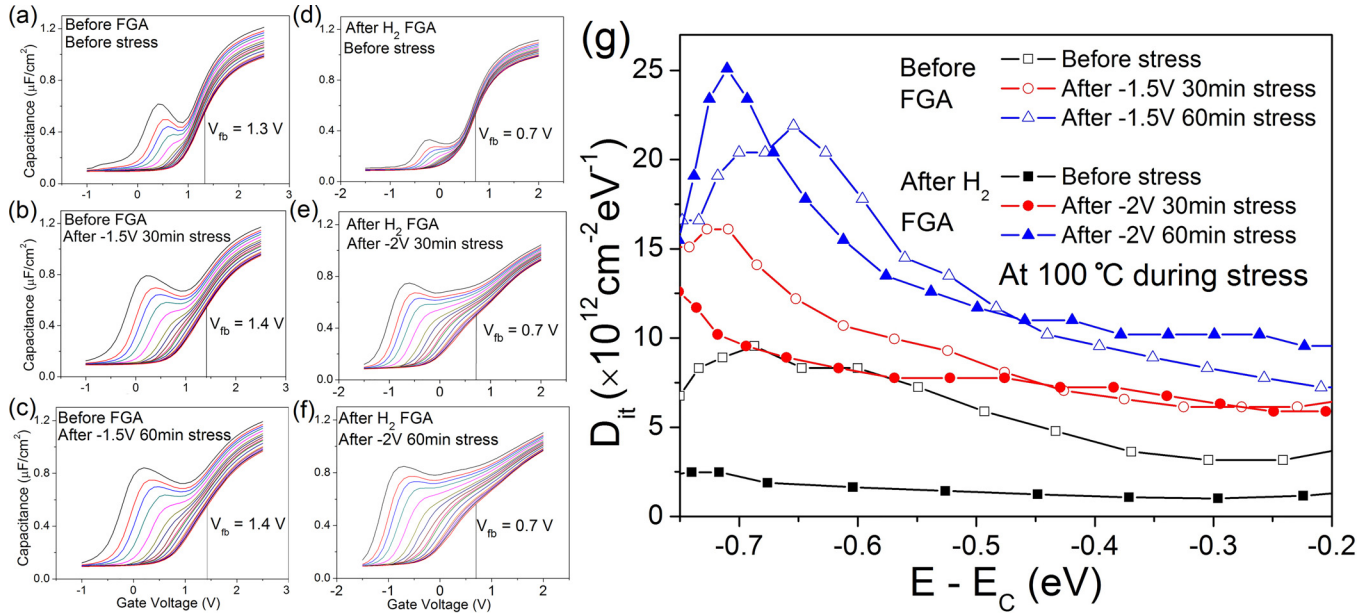

FIG. 2. Negative bias temperature stress for as-deposited and post-FGA Al_2O_3/InGaAs gate stacks. (a)–(c) Room temperature multi-frequency C-V measurements of as-deposited Al_2O_3/InGaAs after 0, 30, and 60 min of electrical stressing at 100 °C. (d)–(f) Room temperature C-V measurement for post-FGA Al_2O_3/InGaAs after 0, 30, and 60 min of electrical stressing at 100 °C. (g) Extracted D_{it} for all the samples in (a)–(f).

much less than that observed for the post-FGA samples [Figs. 2(d)–2(f)]. It is interesting to note that while the size of inversion bump is much smaller for the post-FGA samples compared to pre-FGA ones before the BTS test [Figs. 2(a) and 2(d)], upon extending the BTS time to 30 min and further to 60 min, the frequency dispersion of the inversion capacitance becomes increasingly similar for the two types of samples [Figs. 2(b), 2(c), 2(e), and 2(f)]. This observation indicates that the interface quality of pre-FGA and post-FGA gate stacks converges during the extended BTS test, which is also supported by the extracted D_{it} in Fig. 2(g). From this D_{it} summary plot, an improvement of the D_{it} occurs during the FGA, but this improvement is negated by the BTS test, producing similar D_{it} for the pre-FGA and post-FGA samples with increasing biasing time. Because the main effect of FGA on the interface is the passivation of charge traps by exposure to atomic hydrogen,[12,13] the offset of this improvement suggests that the BTS treatment may have the opposite effect, causing atomic hydrogen to depassivate from the dangling bonds at the interface under electric field stress. This is consistent with the BTS-induced degradation of the interface quality, especially for those samples tested after FGA.

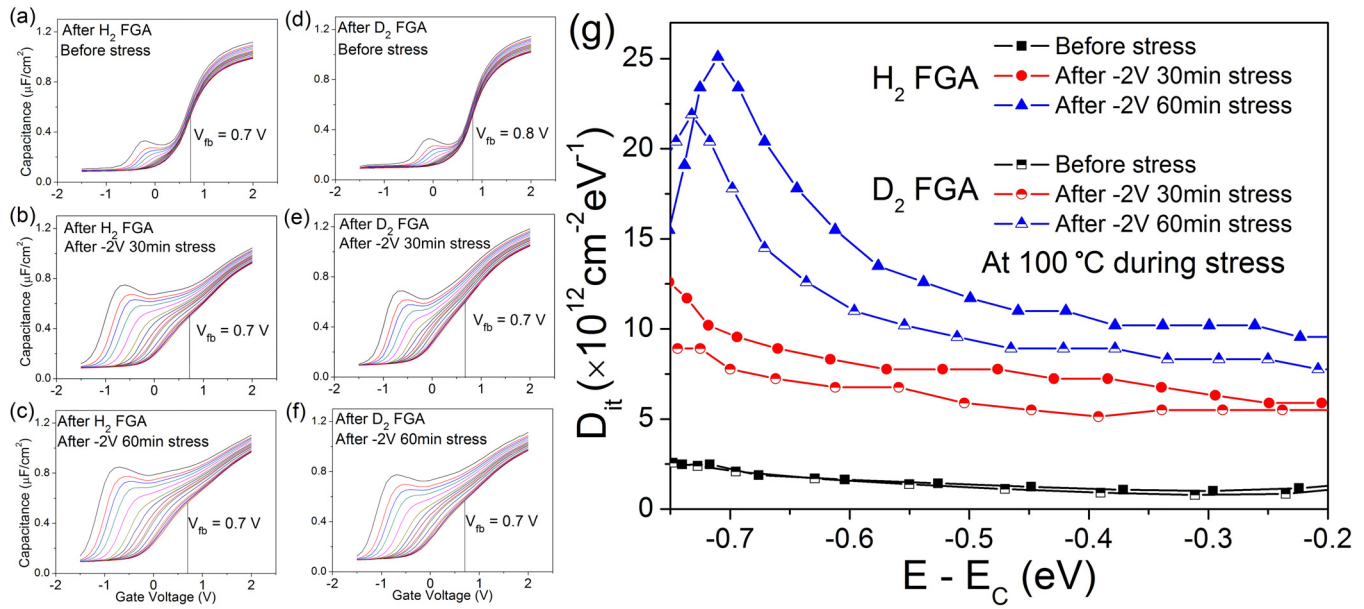

FIG. 3. Comparison of H_2 and D_2 FGA treated Al_2O_3/InGaAs gate stacks with negative bias temperature stress. (a)–(c) Room temperature C-V measurements of H_2 FGA treated Al_2O_3/InGaAs after 0, 30, and 60 min of electrical stressing at 100 °C. (d)–(f) Room temperature C-V measurements of D_2 FGA treated Al_2O_3/InGaAs after 0, 30, and 60 min of electrical stressing at 100 °C. (g) Extracted D_{it} for all the samples in (a)–(f).

A hydrogen isotope experiment was employed to probe the hydrogen depassivation mechanism during BTS. Deuterated FGA was performed on Al_2O_3/InGaAs after the metallization process under conditions identical to those used for the regular post-gate H_2/N_2 FGA. While the similarity between the C-V curves in Figs. 3(a) and 3(b) indicates an almost identical initial passivation of D_{it} and N_{bt} by H_2/N_2 FGA and D_2/N_2 FGA, a notable difference is observed in the device response after BTS is performed. Under the same BTS test conditions, the gate stacks fabricated using deuterated FGA show a smaller capacitance dispersion in inversion than those made by the regular H_2/N_2 FGA [Figs. 3(b)–3(f)], and a lower extracted D_{it}, as displayed in Fig. 3(g). This difference is reproducible for numerous MOS capacitors (MOSCAPs) of different gate areas prepared on each sample. This is a clear sign of a hydrogen isotope effect, suggesting that the mass difference of H and D affects the BTS induced interface degradation in Al_2O_3/InGaAs devices, consistent with the idea of slower field-driven depassivation of defects by deuterium than by hydrogen. Such an isotope effect has been reported previously for Si devices,[38,39] and is interpreted as a strong indicator of a hydrogen desorption/depassivation mechanism as the cause of degraded device reliability.

To further elucidate that the higher sensitivity to BTS for the post-FGA samples compared to un-annealed ones results from hydrogen depassivation, rather than a simple thermal annealing effect during the FGA, we fabricated another set of samples by annealing the post-metallization Al_2O_3/InGaAs gate stacks in purified N_2 with the same thermal budget used during FGA (400 °C for 30 min). The N_2 passes through a gettering furnace to scavenge O_2 before entering a quartz tube furnace for sample annealing, and the concentration of O_2 in the N_2 gas at the outlet of the gettering furnace reads ~0.01 ppm. The C-V data for the N_2 annealed gate stacks is shown in Fig. 4(b). The effect of negative BTS for the N_2 annealed gate stacks [Figs. 4(b) and 4(e)] is compared to that of the un-annealed [Figs. 4(a) and 4(d)] and post-FGA samples [Figs. 4(c) and 4(f)], with identical stressing temperature and a similar applied electric field in the Al_2O_3 dielectric. An increase of the capacitance dispersion in inversion is observed for the N_2 annealed samples after BTS testing. Similar to the un-annealed gate stacks, the N_2 annealed samples show a much smaller magnitude of interface degradation compared to the post-FGA ones. This result is quantitatively illustrated in the D_{it} values extracted by analysis of the C-V data using the full interface state model, as shown in Fig. 4(g). For all these three types of devices, negative BTS induces an increase of the D_{it} across the bandgap. Near the conduction band edge, the increase of D_{it} after negative BTS testing is $\sim 3 \times 10^{12}\,cm^{-2}eV^{-1}$ for both the un-annealed and N_2 annealed devices, and is $\sim 7 \times 10^{12}\,cm^{-2}eV^{-1}$ for the post-FGA samples. This result demonstrates the similar interface degradation behavior of the N_2 annealed Al_2O_3/InGaAs gate stacks compared to un-annealed devices, and their difference from the post-FGA samples. It is evident that the BTS induced interface degradation of post-FGA devices is correlated with the use of hydrogen to passivate interface traps (and their depassivation under stressing), rather than the thermal effect of annealing alone. The mid-gap D_{it} at $E - E_C = -0.37$ eV for all samples measured under various BTS conditions is summarized in Fig. 5.

IV. CONCLUSIONS

In conclusion, we investigated the reliability of Al_2O_3/InGaAs gate stacks through BTS tests. While having a negligible effect on the N_{bt}, BTS testing at 100 °C, especially under negative bias, induces a significant increase in D_{it}. This degradation effect is more significant for the post-FGA devices than the un-annealed samples or those annealed in inert environments. Interface trap passivation during FGA is reversed by the negative BTS testing, causing the post-FGA

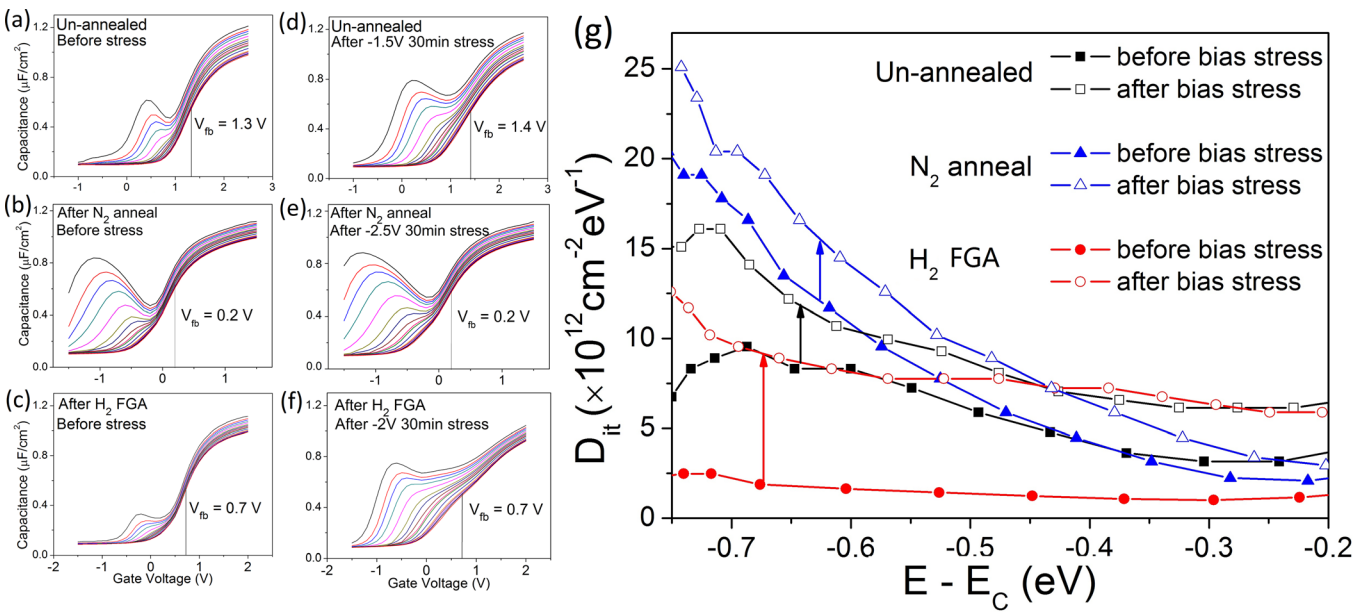

FIG. 4. Negative bias temperature stress for Al_2O_3/InGaAs before FGA, after N_2 anneal, and after H_2 FGA. (a)–(c) Room temperature C-V measurements for pre-bias-stressing Al_2O_3/InGaAs before FGA, after N_2 anneal, and after H_2 FGA. (d)–(f) Room temperature C-V measurements for the above gate stacks after 30 min of electrical stressing at 100 °C. (g) Extracted D_{it} for all the samples in (a)–(f).

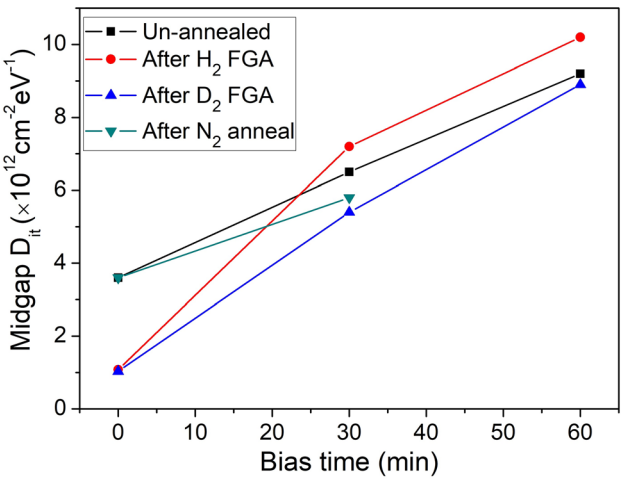

FIG. 5. The mid-gap D_{it} ($E - E_C = -0.37$ eV) for Al_2O_3/InGaAs with various post-metal treatments and BTS times. Details of BTS conditions are applicable to the data in Figs. 2–4.

D_{it} to converge to pre-FGA D_{it} values with increasing BTS time, indicating depassivation of hydrogen from interface defects. This mechanism is further supported by the hydrogen isotope effect, showing improved reliability of Al_2O_3/InGaAs for devices with deuterated FGA compared to H_2/N_2 FGA. This study demonstrates a potentially irrecoverable interface trap increase for post-FGA Al_2O_3/InGaAs gate stacks operating at elevated temperatures, which is caused by hydrogen depassivation from defects at the oxide/semiconductor interface. Further study to improve the thermal and bias stability of hydrogen passivation or explore alternative passivation approaches for a more stable enhancement of oxide/InGaAs device performance is needed to avoid the observed increase in interface state density.

ACKNOWLEDGMENTS

The authors acknowledge support from the Semiconductor Research Corporation through the Non-Classical CMOS Research Center (Task ID 1437.008), the Stanford Initiative in Nanoscale Materials and Processes (INMP), and the US-Israel Binational Science Foundation.

[1]J. A. del Alamo, Nature **479**, 317 (2011).
[2]G. He, B. Deng, H. Chen, X. Chen, J. Lv, Y. Ma, and Z. Sun, APL Mater. **1**, 012104 (2013).
[3]B. Shin, J. R. Weber, R. D. Long, P. K. Hurley, C. G. Van de Walle, and P. C. McIntyre, Appl. Phys. Lett. **96**, 152908 (2010).
[4]G. He, L. Zhu, Z. Sun, Q. Wan, and L. Zhang, Prog. Mater. Sci. **56**, 475 (2011).
[5]Q. Li, X. Zhou, C. W. Tang, and K. M. Lau, IEEE Electron Device Lett. **33**, 1246 (2012).
[6]G. He, X. Chen, and Z. Sun, Surf. Sci. Rep. **68**, 68 (2013).
[7]V. Chobpattana, T. E. Mates, W. J. Mitchell, J. Y. Zhang, and S. Stemmer, J. Appl. Phys. **114**, 154108 (2013).
[8]R. Suzuki, N. Taoka, M. Yokoyama, S. Lee, S. H. Kim, T. Hoshii, T. Yasuda, W. Jevasuwan, T. Maeda, O. Ichikawa, N. Fukuhara, M. Hata, M. Takenaka, and S. Takagi, Appl. Phys. Lett. **100**, 132906 (2012).
[9]J. Ahn, T. Kent, E. Chagarov, K. Tang, A. C. Kummel, and P. C. McIntyre, Appl. Phys. Lett. **103**, 071602 (2013).
[10]H. D. Trinh, E. Y. Chang, P. W. Wu, Y. Y. Wong, C. T. Chang, Y. F. Hsieh, C. C. Yu, H. Q. Nguyen, Y. C. Lin, K. L. Lin, and M. K. Hudait, Appl. Phys. Lett. **97**, 042903 (2010).
[11]L. Yueh-Chin, H. Mao-Lin, C. Chen-Yu, C. Meng-Ku, L. Hung-Ta, T. Pang-Yan, L. Chun-Hsiung, C. Hui-Cheng, L. Tze-Liang, L. Chia-Chiung, J. Syun-Ming, H. D. Carlos, H. He-Yong, S. Yuan-Chen, and C. Edward Yi, Appl. Phys. Express **7**, 041202 (2014).
[12]E. J. Kim, L. Wang, P. M. Asbeck, K. C. Saraswat, and P. C. McIntyre, Appl. Phys. Lett. **96**, 012906 (2010).
[13]K. Tang, R. Winter, L. Zhang, R. Droopad, M. Eizenberg, and P. C. McIntyre, Appl. Phys. Lett. **107**, 202102 (2015).
[14]J. R. Weber, A. Janotti, and C. G. Van de Walle, J. Appl. Phys. **109**, 033715 (2011).
[15]T. D. Lin, W. H. Chang, R. L. Chu, Y. C. Chang, Y. H. Chang, M. Y. Lee, P. F. Hong, M.-C. Chen, J. Kwo, and M. Hong, Appl. Phys. Lett. **103**, 253509 (2013).
[16]T. D. Lin, Y. H. Chang, C. A. Lin, M. L. Huang, W. C. Lee, J. Kwo, and M. Hong, Appl. Phys. Lett. **100**, 172110 (2012).
[17]M. Hong, H. W. Wan, K. Y. Lin, Y. C. Chang, M. H. Chen, Y. H. Lin, T. D. Lin, T. W. Pi, and J. Kwo, Appl. Phys. Lett. **111**, 123502 (2017).
[18]J. Lin, Y. Y. Gomeniuk, S. Monaghan, I. M. Povey, K. Cherkaoui, É. Connor, M. Power, and P. K. Hurley, J. Appl. Phys. **114**, 144105 (2013).
[19]K. Tang, F. R. Palumbo, L. Zhang, R. Droopad, and P. C. McIntyre, ACS Appl. Mater. Interfaces **9**, 7819 (2017).
[20]J. Franco, B. Kaczer, A. Vais, A. Alian, H. Arimura, V. Putcha, S. Sioncke, N. Waldron, D. Zhou, and L. Nyns, MRS Adv. **1**, 3329 (2016).
[21]M. F. Li, G. Jiao, Y. Hu, Y. Xuan, D. Huang, and P. D. Ye, IEEE Trans. Device Mater. Reliab. **13**, 515 (2013).
[22]D. K. Schroder, Microelectron. Reliab. **47**, 841 (2007).
[23]X. Gong, B. Liu, and Y. C. Yeo, IEEE Trans. Device Mater. Reliab. **13**, 524 (2013).
[24]J. Franco, A. Alian, B. Kaczer, D. Lin, T. Ivanov, A. Pourghaderi, K. Martens, Y. Mols, D. Zhou, N. Waldron, S. Sioncke, T. Kauerauf, N. Collaert, A. Thean, M. Heyns, and G. Groeseneken, in *IEEE International Reliability Physics Symposium Proceedings* (2014), p. 6A.2.1.
[25]F. Palumbo, I. Krylov, and M. Eizenberg, J. Appl. Phys. **117**, 104103 (2015).
[26]G. F. Jiao, W. Cao, Y. Xuan, D. M. Huang, P. D. Ye, and M. F. Li, in *IEEE International Electron Devices Meeting* (2011), p. 27.1.1.
[27]F. Palumbo and M. Eizenberg, J. Appl. Phys. **115**, 014106 (2014).
[28]A. Vais, K. Martens, J. Franco, D. Lin, A. Alian, P. Roussel, S. Sioncke, N. Collaert, A. Thean, M. Heyns, G. Groeseneken, and K. DeMeyer, in *2015 IEEE International Reliability Physics Symposium* (2015), p. 5A.7.1.
[29]G. Jiao, C. Yao, Y. Xuan, D. Huang, P. D. Ye, and M. F. Li, IEEE Trans. Electron Devices **59**, 1661 (2012).
[30]K. Tang, R. Droopad, and P. C. McIntyre, ECS Trans. **69**, 53 (2015).
[31]K. Tang, A. C. Meng, R. Droopad, and P. C. McIntyre, ACS Appl. Mater. Interfaces **8**, 30601 (2016).
[32]J. Ahn, B. Shin, and P. C. McIntyre, ECS Trans. **45**, 183 (2012).
[33]H. P. Chen, Y. Yuan, B. Yu, J. Ahn, P. C. McIntyre, P. M. Asbeck, M. J. W. Rodwell, and Y. Taur, IEEE Trans. Electron Devices **59**, 2383 (2012).
[34]Y. Yuan, B. Yu, J. Ahn, P. C. McIntyre, P. M. Asbeck, M. J. W. Rodwell, and Y. Taur, IEEE Trans. Electron Devices **59**, 2100 (2012).
[35]R. Engel-Herbert, Y. Hwang, and S. Stemmer, Appl. Phys. Lett. **97**, 062905 (2010).
[36]R. Winter, J. Ahn, P. C. McIntyre, and M. Eizenberg, J. Vac. Sci. Technol. B **31**, 030604 (2013).
[37]J. Huang, N. Goel, H. Zhao, C. Y. Kang, K. S. Min, G. Bersuker, S. Oktyabrsky, C. K. Gaspe, M. B. Santos, P. Majhi, P. D. Kirsch, H. H. Tseng, J. C. Lee, and R. Jammy, in *2009 IEEE International Electron Devices Meeting (IEDM)* (2009), p. 1.
[38]K. Hess, I. C. Kizilyalli, and J. W. Lyding, IEEE Trans. Electron Devices **45**, 406 (1998).
[39]Z. Chen, K. Hess, J. Lee, J. W. Lyding, E. Rosenbaum, I. Kizilyalli, S. Chetlur, and R. Huang, IEEE Electron Device Lett. **21**, 24 (2000).