MEASUREMENT OF THERMAL CONDUCTIVITY OF GOLD NANOFILMS AND NANOWIRES

by

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As I wrote my master's thesis many years ago, I listened to my Talking Heads albums over and over, so it only seems fitting that I include this lyric in my acknowledgements: "And you may ask yourself, well, How did I get here?" Throughout my life, I asked the question, "how *did* I get here?" as my family traveled across the country, raising children, living in new communities, and working in different places. Yet, as I ask myself this question now (during a global pandemic!), I know the answer. I got here, in large part, through the love, kindness, friendship, help, and support of many wonderful people. I'd like to acknowledge them now.

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LIST OF ABBREVIATIONS

Abbreviation	Description
AFM	Atomic Force Microscope
ALD	Atomic Layer Deposition
AMD	Advanced Micro Devices
BOBYQA	Boundary Optimization by Quadratic Approximation
BTE	Boltzmann Transport Equation
CAD	Computer-aided Design
CDA	Clean Dry Air
CNTFET	Carbon Nanotube Field Effect Transistor
CVD	Chemical Vapor Deposition
DUT	Device Under Test
EBL	E-beam Lithography
EUVL	Extreme Ultraviolet Lithography
FDTR	Frequency Domain Thermoreflectance
FEA	Finite Element Analysis
FEBID	Focussed Electron Beam Induced Deposition
FinFET	Fin Field Effect Transistor
GAAFET	Gate All Around Field Effect Transistor

GIS	Gas-Injection System
HV	High Vacuum
IC	Integrated Circuit
IoT	Internet of Things
IPA	Isopropyl Alcohol
ITRS	International Technology Roadmap for Semiconductors
Kn	Knutsen Number
MFP	Mean Free Path
MIBK	Methyl Isobutyl Ketone
MMA	Methyl Methacrylate
MW	Molecular Weight
NPGS	Nanoscale Pattern Generation System
PMMA	Polymethyl Methacrylate
PVD	Physical Vapor Deposition
RC	Resistance-Capacitance
RIE	Reactive-Ion Etch
RMS	Root Mean Square
RTD	Resistive Temperature Device
SAM	Self-assembled Monolayer

SEM	Scanning Electron Microscope
SSTR	Steady State Thermoreflectance
SThM	Scanning Thermal Microscopy
TBR	Thermal Boundary Resistance
TCR	Temperature Coefficient of Resistance
TDTR	Time Domain Thermoreflectance
TIFF	Tagged Image File
TIM	Thermal Interface Material
TPF	Two Photon Fluorescence
TSMC	Taiwan Semiconductor Manufacturing Company
TTR	Transient Thermoreflectance
UHV	Ultra-high Vacuum
UV	Ultraviolet
XRR	X-ray Reflectivity

ABSTRACT

Achieving complex integrated circuits and devices, through miniaturization into the nanoscale, increasingly relies on understanding the thermal properties of the materials used in these components. Conductors at the nanoscale have properties that differ substantially from their bulk or thin film counterparts. Nanostructured gold, for example, is currently being used in a wide range of applications, including interconnects, solar cells, flexible screens, detection of cancerous cells, and energy storage. Thermal management on the nanoscale has posed significant industry challenges that directly impact the maximum current and power, speed, reliability, and lifetime of devices where so-called self-heating is a factor. General factors at reduced scale include increasing resistivity, reduction in thermal conductivity (κ), and the desired increasing device density per unit area. Despite the prominent role of metallic nanostructures in current and future technologies, large gaps exist in understanding the influence of "size effects" on thermal characteristics at small dimensions. Prior work attempted to simulate the thermal characteristics of nanoscale materials to account for these size effects, but often fall short due to the lack of experimental verification needed for informing and testing the models based, primarily, on the Boltzmann transport equation.

This dissertation focuses on development and test of a method used to generate direct experimental data on κ for nanofilms and nanowires. The approach is applied to gold with thickness dimensions of 50 and 100 nm. The lateral dimensions studied range

from 74 nm to 720 nm, thereby spanning the micro to nano regimes. The main components of this research are the fabrication and measurement methodology for direct studies of thermal conductivity at the nanoscale. Both design and data analysis rely on extensive finite element analysis simulations.

The experimental results include an observed decrease in thermal conductivity as film thickness is reduced, for any lateral dimension studied. At large lateral width, corresponding to the microscale, κ values are 280 and 200 W/mK for thicknesses of 100 and 50 nm, respectively. These are to be compared with the accepted value of 317 W/mK for κ of bulk gold. In addition, as the latter is reduced, for either thickness, a characteristic decrease is observed beginning at ~300 nm width. For the smallest nanowire investigated, 50 nm in thickness and 74 nm in width, a value of κ = 56 W/mK is obtained. The trends obtained are supported by data available in the literature. The decrease in κ with diminishing size are also consistent with theoretical calculations for gold, thereby validating the reported Boltzmann transport equation approach.

1. INTRODUCTION

The evolution of nanoscale technologies and the Internet of Things (IoT) continues to drive enormous change within the semiconductor industry.[12] The term IoT refers to the interconnection of multiple computing devices designed to send and receive data, and to interface without direct human involvement. As shown in Figure 1, the combined market of IoT will increase to approximately $520 billion in 2021, with worldwide technology spending reaching $1.2T in 2022 [3, 13] The proliferation of "smart devices" is not confined to industrialized countries. Such devices play a critical role in developing countries as well, contributing to transportation safety, agriculture, environment monitoring, utilities management, health care management, etc. [14] These devices truly bridge the gap between the physical and digital worlds.

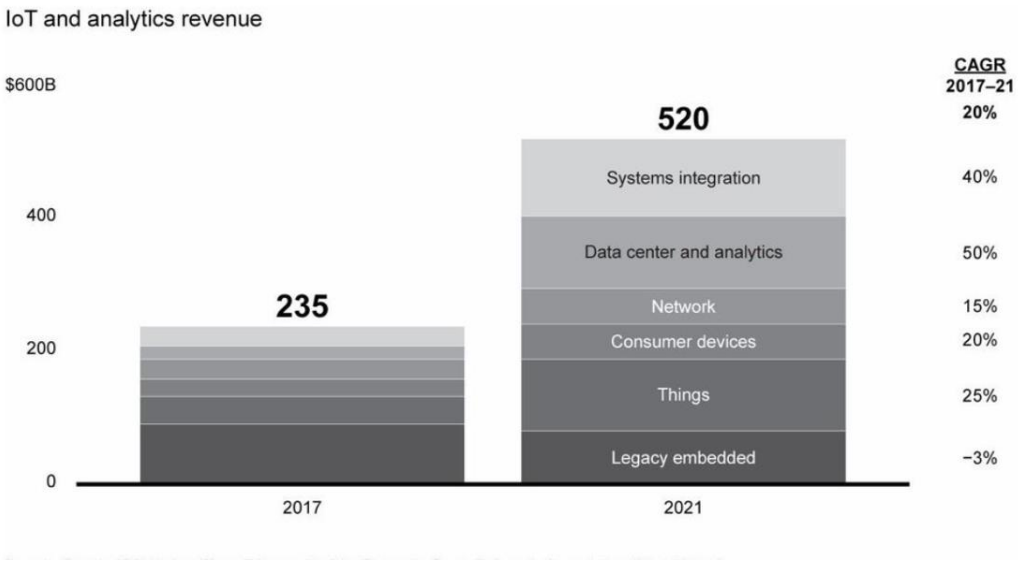


Figure 1. Growth of Combined Markets of the Internet of Things. [3]

Key to this evolution is "technology scaling," which refers to both the miniaturization in physical dimensions of components as well as the reduction in supply

voltage to reduce power dissipation and maintain reliability [15, 16]. The emphasis on scaling has been a predominant focus of the industry for many years, as device requirements include increased functionality and reliability, while maintaining lighter weights and smaller packages. In 1965, co-founder of Intel, Gordon Moore predicted that the number of components that would economically fit on a chip for a commercial, high volume manufacturer would double every year.[17] Commonly known as Moore's Law, the prediction was later revised in 1975 to adjust the pace to doubling every 2 years. While changes in wafer size and chip architectures facilitated the validity of Moore's prediction, it is the exponential decrease in feature size over the past 50 years that has represented some of the most innovative advancements in chip manufacture. In this case, feature size refers to parameters such as gate insulator thickness, channel length, and distance between closest interconnect. [18] Miniaturization of components allows for

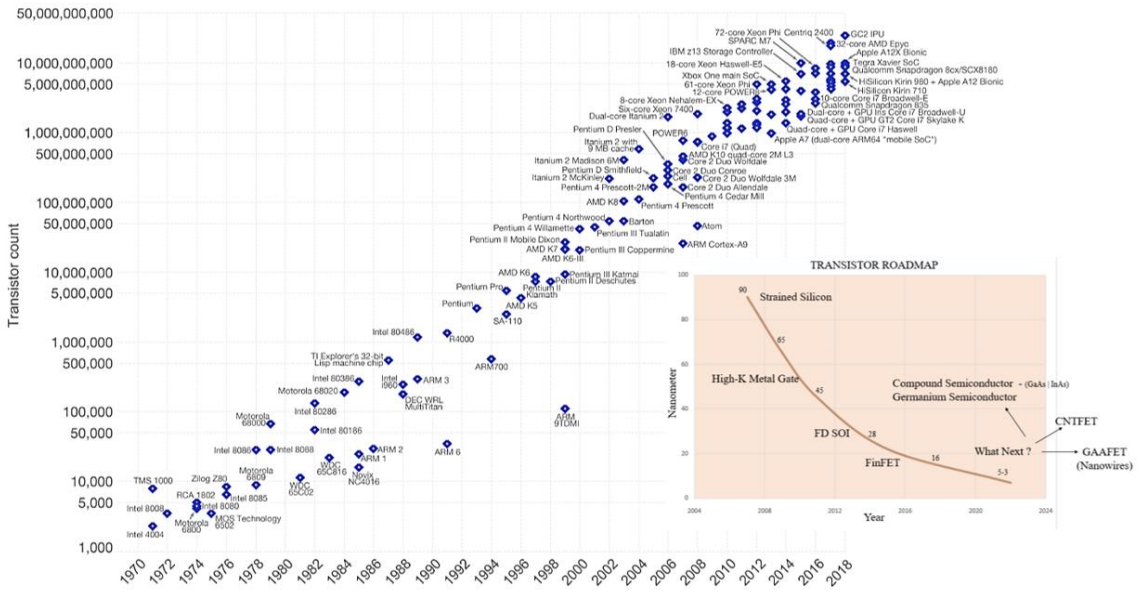


Figure 2. Moore's Law and ITRS Roadmap.

improved circuit speeds, lighter weights and potentially lower costs, allowing for the world-wide prevalence of electronic devices.

Figure 2 illustrates the realization of Moore's law, with the number of transistors on integrated circuit (IC) chips over time, from 1971-2018.[19] The inset in the figure presents the corresponding node size (in nanometers) over time from 2004 extending to 2024. [20] Included in this "transistor roadmap," is the associated technologies beginning with strained silicon at 90nm in 2006, to FinFET at 16nm in 2016. Advanced technologies including CNTFET, compound semiconductors, and GAAFET are believed to extend the technology 3-5nm node in the future. The continued march along the trajectory of Moore's law has slowed in recent years.[21] For example, Intel introduced a 14-nm node technology in 2014, but the anticipated 10-nm node benchmark stalled until late 2019 with limited release. [20] Samsung, Apple, TSMC, and AMD also continue to advance towards the 7-nm node, but at decidedly slower pace than Moore's Law dictates. [21]

1.1 Challenges

Miniaturization of devices such as integrated circuits, microprocessors, and light-emitting diodes presents significant technical challenges. These challenges include thermal management, nanofabrication fidelity, metrology capabilities, and material limitations. Miniaturization results in higher power densities, causing substantial heating or "hot spots" within the device.[22] Heating is a result of energy loss when current densities are high, such as in cases where there is current crowding. The heat produces a temperature rise which may cause changes in material properties (e.g. conductivity), local thermal stresses, and other undesirable issues. If the heat is not properly dissipated into

surrounding materials, the hot spots rise in temperature until device failure from melted or shorted wires. Numerous researchers have reported that thermal conductivity also decreases at the nanoscale so that heat flow is impeded, as reviewed by Biele *et al.* and references therein [23]. Zhuo *et al.* conducted studies using thermal microscopy *in situ* to understand the behavior of the metal tracks in ICs under cyclic power conditions. [5] The images shown in Figure 3 illustrate time-lapse mapping highlighting the formation of a hot spot in various metal track configurations over time. Increased incidents of hot spots are evident in bent wires (b), thin wires (c), and damaged wires (d).

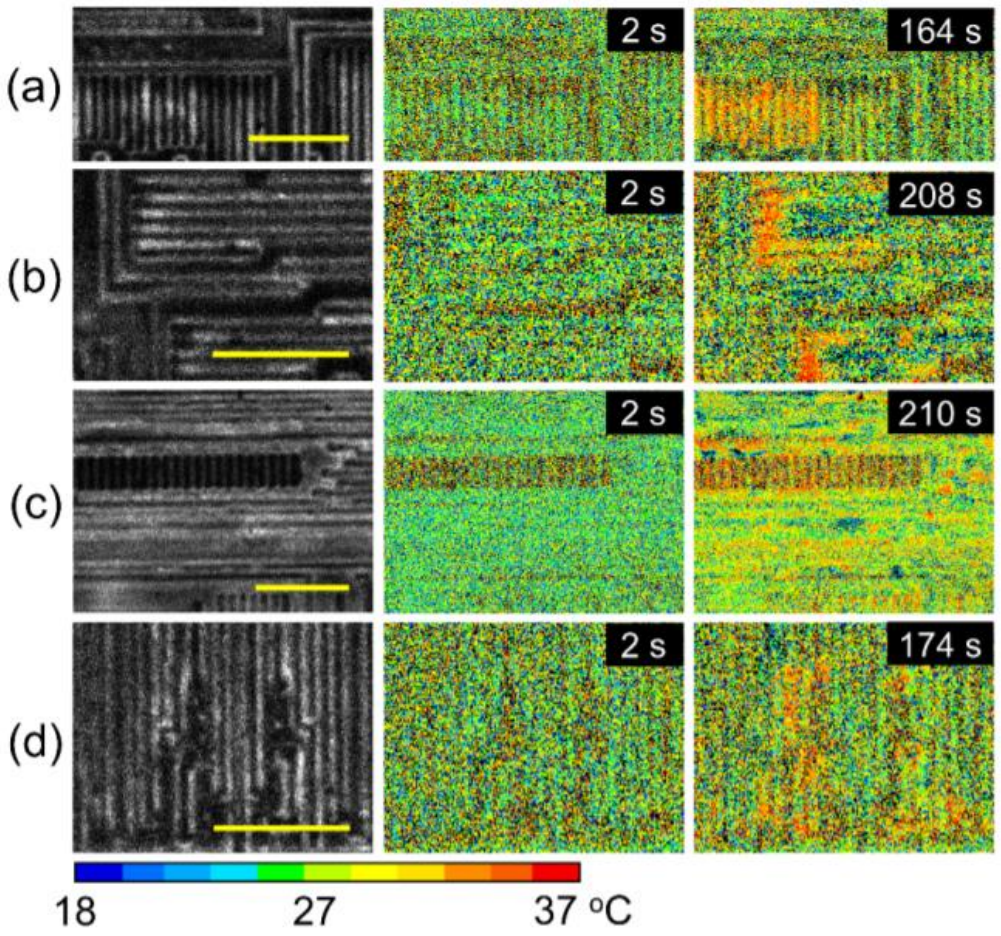


Figure 3.Two-photon fluorescence (TPF) mapping of IC circuitry.
(a) typical metal tracks., (b) metal tracks with bend, (c) thin metal tracks, (d) damaged tracks [5]

Thermal management may take the form of careful material selection, introduction of thermal interface materials (TIM) as heat sinks/spreaders, or external cooling systems. If the thermal load created by hot spots in not adequately addressed, the device may fail or the operation of the device may be throttled down to reduce power. Many chip failures can be attributed to temperature-dependent mechanisms, such as Joule heating and electromigration.[24]

The effectiveness of any thermal management strategy is an understanding of the thermal conductivity of the materials involved. [22] On a macroscopic scale, Fourier's law describes conductive heat transfer through a solid, given by the equation

$$\vec{q} = -\kappa \nabla \mathrm{T} \tag{1}$$

where $\vec{q}$ is the local heat flux vector, ∇T is the local temperature gradient, and κ is thermal conductivity which describes how easily the heat carriers travel through the material.[25]

The mean free path (MFP) is a critical parameter in understanding heat transport in materials. In bulk metals, MFP is the distance an energy carrier, primarily electrons, travels prior to collisions with phonons, impurities, and crystalline defects. [26]

However, when the aforementioned feature size is reduced to the scale of the intrinsic MFP of the heat carriers, additional sources of carrier scattering from external surfaces and grain boundaries suppress the thermal conductivity relative to bulk values. Such suppression promotes the additional formation of hot spots and resultant device failures. Indeed, the industry trend towards the 10 nm to 7 nm nodes is considerably smaller than the mean free path most materials used in devices, resulting in diminished performance, including resistance-capacitance (RC) signal delay [26-28].

An additional challenge to thermal management lies with multiple, heterogeneous material interfaces within devices and the associated increased number of interfaces and boundaries. Boundary layers and interfaces can impede heat flow and further enhance hot spots. The thermal boundary interface can be characterized by the following expression

$$J = G_k \Delta T \tag{2}$$

where J is the heat current at the interface, G_k is the interface conductance, also known as the Kapitza conductance, and ΔT is the temperature discontinuity at the interface.[29, 30] The Kapitza conductance is the result of scattering of heat carriers at interfaces, either between metal layers in devices or between a metal layer and a substrate.

Numerous industries are dependent on nanoscale thermal transport beyond conventional chip manufacturers. High power electronic devices, nanoparticles for medical therapies, light-emitting diodes, flexible electronics, solar cells, and thermoelectric materials rely on the ability of materials to dissipate or confine thermal energy. [31]

Nanofabrication and nanomanufacturing also poses considerable challenges in pursuit of technology scaling. Even small, random variations in a pattern, known as stochastic effects, can create large variations in pattern fidelity, which impacts device performance. [32]

Conventional immersion lithographic processes present a limiting factor to the allowable size of devices and the required precision of patterning.[32] Modifications to photoresist chemistry and mask design have contributed greatly to the ability to achieve small features sizes. However, regardless of these advances, the ability to pattern features smaller than the wavelength of the exposing radiation remains an enormous technical

hurdle in photolithography. Extreme ultraviolet lithography (EUVL) attempts to address this concern with a wavelength of 13.5 nm, but challenges remain to determine suitable resist chemistry and mask design, along with added costs in manufacturing.

Other top-down processes are capable of achieving extremely small feature sizes, including nanoimprint technology and e-beam lithography. E-beam lithography (EBL) will be discussed in detail later in this document. Unfortunately, both processes have very low throughput, rendering them impractical for large-scale production.

Another important factor in technology scaling is metrology. It is estimated that for some products, over 50% of manufacturing steps require some form of measurement or characterization.[33] Moreover, the tighter tolerances of small feature sizes necessitate enhanced inspection protocols and contamination controls, particularly in components that are difficult to physically access with instrumentation. Statistical controls for dimensional, compositional, surface, and interfacial properties must be established within the measurement capability and resolution of a given instrument.

Finally, key material properties, beyond thermal properties, must be optimized for service in electronic devices, including electrical conductivity, melting point, resistance to oxidation, and diffusion kinetics.

Nanoscale materials present significant challenges in terms of both material properties and integration for materials such as aluminum and copper, typically used in commercial applications.[34] Aluminum and, to a lesser extent, copper react with oxygen to form an oxide layer that inhibits electrical and thermal transport. Further, copper readily diffuses through silicon dioxide causing device failures, so a barrier layer is necessary to prevent this behavior. Yet, this barrier layer adds dimension to the device,

antithetical to the trend towards miniaturization. Both aluminum and copper metallization have been extensively used for many years for circuit fabrication using integration processes such as damascene or reactive ion etching. [35] Aluminum interconnects are formed using subtractive reactive ion etch (RIE) process, while copper employs a damascene process due to the unavailability of dry etch plasma chemistry to effectively generate a pattern. Redundant layers and liners are added to the integration to address the aforementioned adhesion and diffusion concerns of the respective materials. Metal deposition techniques, such as physical vapor deposition (PVD), chemical vapor deposition (CVD) or atomic layer deposition (ALD), can potentially provide barrier integration, but require excellent conformity to prevent seam lines and voids from forming.

The required barriers and liners for copper metallization pose significant limitations to scaling to reduced nodes. Scaled liners and barriers result in metal drift, where ionized metal travels through the dielectric due to electric fields, causing leakage and dielectric breakdown.[36, 37]

1.2 Opportunities

The advancement of nanoscale materials has permeated many scientific disciplines and applications. The vast array of technologies spanning different scientific fields is illustrated in Figure 4.[1] Understanding the unique properties of materials on the nanoscale provides opportunities to explore new technologies and applications.

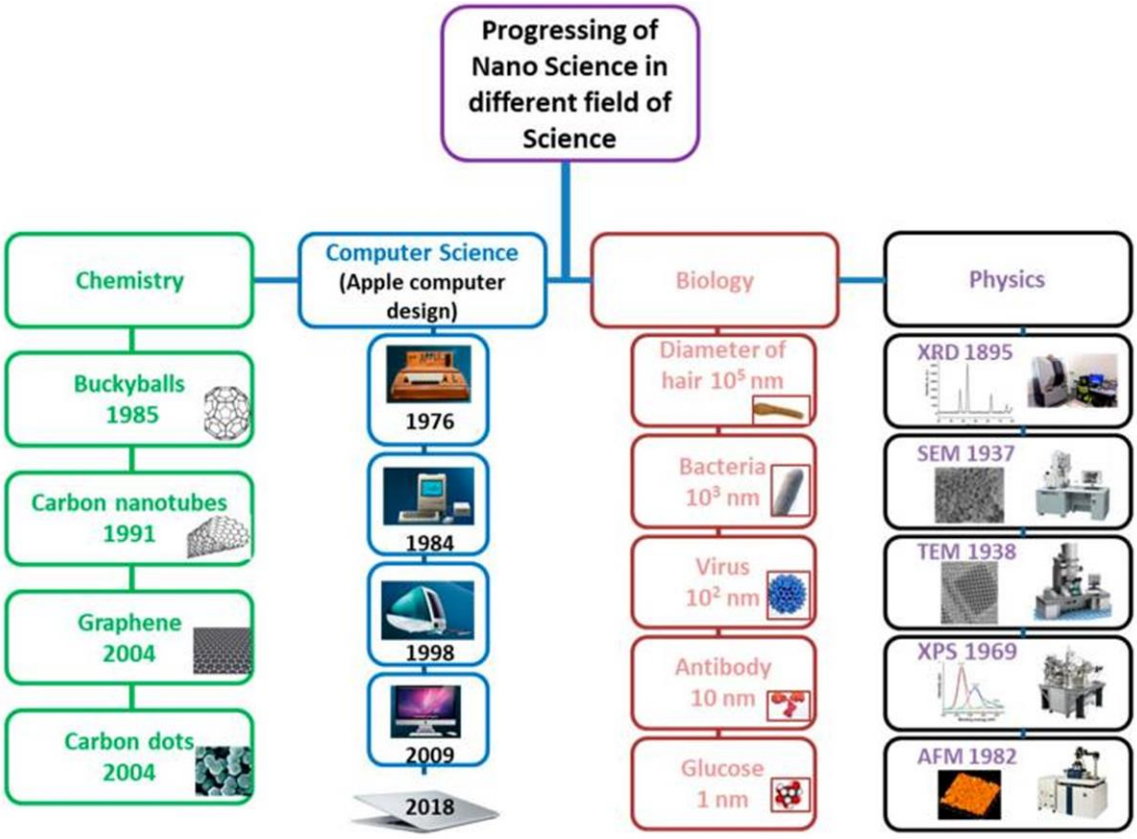


Figure 4. Progress of Nanomaterials. [1]

While a great deal of research concerns thermal management and overcoming the inherent challenges of nanoscale thermal transport, opportunities also exist to exploit this behavior. For example, thermoelectric materials involve the conversion of heat to electrical energy. Quantum-confinements effects of nanostructured materials, coupled with multiple internal interfaces, are optimized so that the thermal conductivity of the device is suppressed without appreciable degradation of electrical transport.[23] Both the use of inclusions within the nanomaterials as well as nanocomposite assemblies have been successful in promoting the thermoelectric effect. The efficacy of a thermoelectric material is quantified by a dimensionless value, the figure of merit ZT, given as:

$$ZT = S^2\sigma T/\kappa \quad (3)$$

where S is the Seebeck coefficient, σ is electrical conductivity, T is temperature, and κ is thermal conductivity.

The properties of S, σ, and κ are interrelated in conventional 3-D crystalline systems, so it is difficult to optimize the material properties independently to affect ZT. [38] In metallic materials, one such interdependent relationship is between electrical and thermal conductivity, the so-called Wiedemann-Franz law which will be discussed in Chapter 2.

Power generation from thermoelectric devices shows great promise in harvesting energy in areas such as solar energy, automotive, industrial heat sources, and even body temperature. [39]

Specifically, many interesting advances of nanoscale thermal transport related to technology scaling is biomedical applications. [40] Advances in IC technology has led to increased functionality of low-powered, implantable medical devices. These small devices can be implanted using minimally invasive procedures to provide drug delivery, monitoring, and disease treatment.[41] Biomedical implants are used in a variety of different applications in areas including ophthalmology (retinal implants), cardiology (stents, grafts, valves), orthopedics (bone grafts, fusion), immunology, and general medicine. Given the limitations of battery capacity, energy harvesting from human body heat or human (vibrational) activity presents a unique opportunity for power management of implantable devices, resulting in improved reliability with minimal impact on the user's lifestyle.

Along with applications in microelectronic devices, the physical and chemical

properties of gold nanoparticles are frequently used in biomedical applications, including therapeutics, diagnostics, drug delivery, and thermal treatments.[42] The high surface to volume ratio of gold nanoparticles allows for surface modification with different functional groups, such as thiols, phosphines, and amines. These modified gold "nanoconjugates" can readily enter living cells to provide site-specific delivery of anti-cancer drugs or other targeted treatments such as laser ablation of tumors.[43]

Finally, flexible electronics represent another frontier to exploit the unique thermal transport properties of nanoscale materials through energy harvesting. [44] Devices that can bend, fold, twist, and stretch have given rise to numerous wearable electronics. Human motion-related applications of flexible/stretchable electronics include self-powered sensors from nanogenerators woven into textiles and triboelectric generators that can drive personal electronic devices.[45] Military applications for wearable thermoelectrics could provide cooling of protective suits and environmental control within armored vehicles. Integration of thermoelectrics in clothing requires specific features including lightweight, waterproof, bendable, washable, and heat resistance. [46]

1.3 Research Focus

Despite the prominent role of metallic nanostructures in current and future technologies, large gaps exist in understanding and measuring thermal characteristics at small dimensions. Morphology, defects, and grain boundaries also play an important role as scattering sites within a nanostructured material that, in turn, affect thermal properties.

There are very few direct measurements of nanoscale thermal conductivity, forcing designers to make educated guesses based on theory and predictive models. In

metallic systems, the critical role of phonons in heat transport has been acknowledged and models have been created to help elucidate the energetics within polycrystalline materials. [47, 48] Yet, challenges still exist as smaller nodes are pursued and driven by multiple markets. Such challenges include the design of viable test structures, fabrication, metrology, analysis of results, and the extraction of meaningful understanding of the measured responses. The generation of empirical data on nanostructured materials remains a difficult endeavor, but such data are critical. Testing must be conducted with methods that achieve the required spatial resolution at the nanoscale and that electrically and thermally isolate the interrogated materials to limit parasitic losses. Careful investigation must also include evaluating material deposition parameters, substrate characteristics, and thermal history of the materials in question to correlate microstructure and morphology with nanoscale thermal behavior.

In this dissertation, the thermal response of a nanostructured gold has been investigated. A series of samples was generated representing a range of dimensions and deposition thicknesses. 50 nm and 100 nm thick nanowires were studied, ranging in width from 74 nm to 280 nm as well as nanofilms, relevant to the diverse applications described above. A direct measurement of thermal conductivity was performed based on a significant body of work performed by Stojanovic *et al.* to develop and understand the functionality of the test structure.[47, 49, 50] Modifications to the test structure design and testing methodology were informed by extensive simulation work. Results were analyzed using existing models, as well as finite element analysis parameter estimation to compare measured and simulated results. Finally, results from this study are compared to those found in literature.

Gold was selected as the subject material for several reasons. Gold is ubiquitous in electronic devices due to its excellent conductivity and ability to withstand high current densities.[51] Gold does not oxidize and remains inert under the typical operating conditions of electronics, providing stability and reliability. Unlike many materials, multiple manufacturing and joining processes are viable for gold metallization. However, gold does not readily adhere to oxide surfaces, necessitating an additional material to aid in bonding to the substrate material. A thin layer of chromium or titanium [52] is frequently used for this purpose, but recent work has shown some success with polymeric self-assembled monolayers (SAM) as an adhesion layer. [53] In the present study, the contribution of an adhesion layer to the heat transport across the interfaces was incorporated in the finite element modeling work. Despite the many advantages of using gold in the electronics industry, the price of gold is relatively high compared to other materials. Further, bonding processes involving gold wire and aluminum have been shown to cause the formation of intermetallics, the so-called "purple-plague."[54] These intermetallics can result in degradation of electrical properties at the bonding sites.

1.4 Organization of This Dissertation

In this chapter, the importance of nanoscale research was discussed, with an emphasis on the challenges and opportunities of technology scaling. In chapter two, thermal properties of nanostructured materials are reviewed, including the impact of microstructure and morphology. Chapter three reviews several techniques for measuring thermal behavior on the nanoscale. Chapter four provides an in-depth review of the direct measurement technique developed by Stojanovic *et al*., which serves as the foundation for this experimental research. The fabrication of the test structures and the electrical

testing method are also discussed in Chapter four. Chapter five presents the material characterization of the gold test structures and the computer simulation and optimization efforts. A discussion of results and comparison with published data is published in Chapter six. Finally, a summary of the conclusions is presented in Chapter 7. The usefulness of the testing and modeling techniques are reviewed, and additional studies are suggested. The Appendix contain specific details of fabrication of focused electron beam induced deposition (FEBID) of cobalt nanowires.

2. THERMAL PROPERTIES OF NANOSTRUCTURES

Thermal conductivity is a function of thermodynamic state (i.e., temperature and pressure) and serves as a measure of the heat transfer capability of a material.[55] It can be defined as the thermal energy that is transmitted through a length or thickness under a given temperature gradient. Temperature is an equilibrium concept and its measurement is only valid under thermodynamic equilibrium. Since heat transport requires a temperature gradient, in accordance with Fourier's law, the temperature can be defined at points of local equilibrium. On the nanoscale, such local thermal equilibrium is achieved by scattering events of the heat carriers. Accordingly, the MFP of the heat carriers, as well as structural scattering sites such as grain boundaries, impurities, surfaces, etc., play a critical role in understanding and measuring nanoscale heat transport.

Thermal conductivities in solid materials can range from 0.015 W/mK in aerogel materials to 2000-3000 W/mK in natural diamond [10]. Thermal conductivity can also be temperature-dependent as well as anisotropic, or directional-dependent.

In the previous section, Fourier's law was introduced to describe heat conduction as discussed in Equation [1]. The illustration shown in Figure 5 represents heat flow

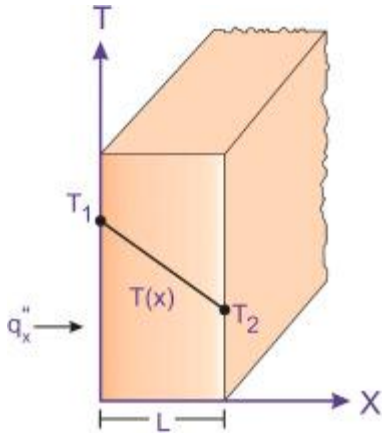


Figure 5. One dimensional Conductive Heat Transfer. [6]

through the thickness (L) of a film, and the resultant temperature gradient. For isotropic situations, thermal conductivity κ may be replaced by a scalar. However, in minute structures, in-plane thermal conductivity can be different than the cross-plane thermal conductivity requiring non-scalar description. [56]. For clarity, there is a distinction between structural anisotropy, which is the result of differences in crystallographic orientation within a material, and nanoscale anisotropy, which is related to variations in material properties due to size and shape dimensions. In addition, variations in polycrystals and grains can also impose yet another anisotropy if they change morphology during deposition or post-processing.

2.1 Mean Free Path (MFP)

As noted in the introduction, the transport properties of nanoscale materials, such as thermal conductivity or electrical resistivity, differ significantly from their bulk counterparts. The free electron model is one way to describe this behavior.[57] In order for an electron to become "free," it must be promoted to one of the empty energy states

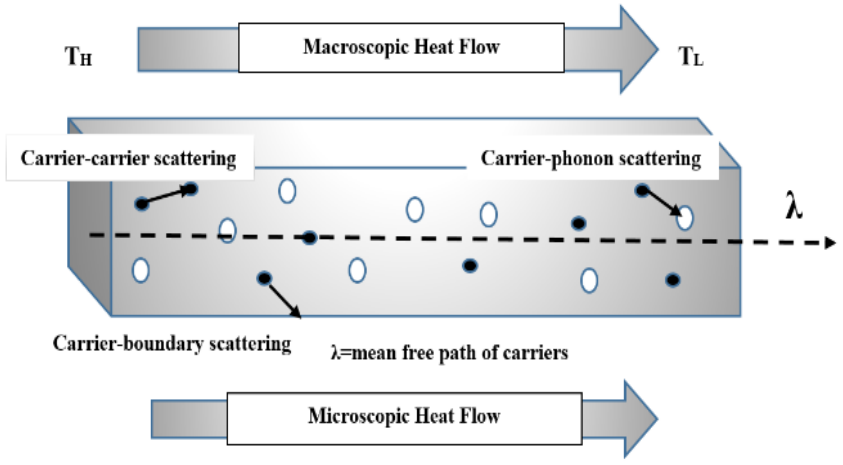


Figure 6. Representation of Nanoscale Carrier Scattering.

above the Fermi energy, E_f.[58] In the early 1900's, Paul Drude theorized that electrons in a solid experience multiple, instantaneous collisions, as illustrated in Figure 6. In metallic systems, the MFP is the average distance the heat carriers, primarily electrons, travel before scattering, and is estimated to be in the range of 4 – 60 nm at room temperature. [26, 59] Drude's model indicates that an electron will travel at a speed for a given time until it scatters, thus changing its energy and momentum. The electron will then travel for an additional period of time before the next scattering event occurs. In very pure metals, such electrons can travel along a straight path for a quite a distance without colliding, often referred to as ballistic conduction. Scattering will only occur when electrons collide with something.

Scattering sources include impurities, vacancies, dislocations, grain boundaries, point defects, and lattice thermal vibrations (phonons). [56] Matthiessen's rule is helpful to understand the additive nature of electron scattering behavior, given as

$$\frac{1}{\tau} = \frac{1}{\tau_1} + \frac{1}{\tau_2} + \frac{1}{\tau_3} + \cdots \tag{4}$$

where τ_j may be the collision times for scattering by phonons, or by imperfections, or by other types of processes. Further, the law dictates that the scattering process is dominated by the shortest scattering rate, so the type of scattering in a specific temperature regime may be predicted. For example, at room temperature, electrical resistivity is the result of collisions between electrons and lattice phonons.[57] At considerably lower temperatures (4K), resistivity is dominated by collisions with impurity atoms and mechanical imperfections within the lattice, and the phonon contribution is negligible. At high temperatures, large number of phonons (lattice vibrations) are present, so the model indicates that scattering will be predominately by phonons, and the contributions of other

forms of scattering will be negligible.

Table 1. Material Properties of Common Electronic Materials

Element		MFP λ_{rt}(nm)	Thermal Conductivity κ(W/mK)	Resistivity ρ(nΩ-m)
Gold	Au	37.7	317	22.14
Silver	Ag	53.3	428	15.87
Copper	Cu	39.9	399	16.78
Aluminum	Al	26.5	237	18.9
Cobalt	Co	11.8/7.77*	100	62
Ruthenium	Ru	6.59/4.88*	117	78
Tungsten	W	15.5	174	52.8

*transport perpendicular and parallel to the hexagonal axis, MFP Ref [26] , κ and ρ Ref [60]

Table 1 presents material properties of several metals commonly used electronic materials. The electronic MFP values were obtained from density functional calculations. [26] When the dimensions of a component approach the MFP, the surface and grain boundaries become critically important scattering sources, thus reducing the thermal conductivity of the material. The scattered electrons cannot pass through the grain boundary, but they can exchange energy with local phonons as they scatter and collide. Phonons can transport through grain boundaries more readily than electrons. [61] Figure 6 illustrates how carriers are scattered by exterior surfaces, by phonons, and by other carriers. This phenomenon is commonly referred to as “size effects” and is a significant barrier to the pursuit of smaller nodes in nanoelectronics.[26] Classical models by Fuchs and Sondheimer [62], and Mayadas and Shatzkes [63] predict the extent to which resistivity increases as a result of electron scattering, based on the Boltzmann transport equation.

It is important to note that these models include the effects of surface specularity and/or grain boundaries present in polycrystalline thin metallic film.[47] These factors

also contribute significantly to the observed reduction in resistivity and thermal conductivity of nanoscale materials as compared to bulk values.

2.2 Wiedemann-Franz Law

As electrons collide with phonons, the Fermi surface (assumed as spherical for this model) is incrementally displaced at a given velocity, leading to the following expression for conductivity σ,

$$\sigma = \frac{ne^2\tau}{m} \tag{5}$$

where e is the electron charge, τ is the scattering rate, n is the number density of electrons, and m is the effective mass of the electron.

Similar to electrical transport, thermal transport is also dependent on the scattering of free electrons with phonons as the heat flux travels from high temperatures to lower temperature. Sommerfeld's model provides a useful description of thermal conductivity κ,

$$\kappa = \frac{1}{6} n\pi^2 k_B^2 (\mathrm{T}/E_F)\, \nu_F^2 \tau \tag{6}$$

where k_b is the Boltzmann constant, E_f is the Fermi energy, T is temperature, and ν_F is the Fermi velocity. Since free electrons are the dominant energy carrier for both electrical and thermal transport in metals, Equations [6] and [7] can be combined, yielding a ratio of thermal conductivity to electrical conductivity known as the Wiedemann-Franz law.

$$L \equiv \frac{\kappa}{\sigma T} = \pi^2/3(k_B^2/e^2) \tag{7}$$

L is known as the Lorenz number. This relationship works well for bulk materials at high and low temperatures, but does not apply in the Debye region, where scattering behavior

is impacted.

Table 2. Experimental Lorenz Values [64]

	L x 10^8 [WΩ/deg^2]	
Metal	0°C	100°C
Gold (Au)	2.35	2.40
Silver (Ag)	2.31	2.38
Copper (Cu)	2.23	2.33
Platinum (Pt)	2.51	2.60
Tungsten (W)	3.04	3.20

The usefulness of the Wiedemann-Franz law stems from the fact that direct measurement of thermal conductivity is very difficult. Electrical conductivity is an easier value to determine empirically, due to the ability to adequately achieve electrical isolation of structures as compared to thermal isolation [50]. The law serves as an approximation of thermal conductivity, but there are significant limitations on its validity for nanoscale materials. On the nanoscale, the law assumes that a decrease in electron mobility due to size effects should impact thermal conductivity and electrical resistivity to the same extent, but that is not the case. [65] At low dimensions, the contribution of phonon thermal conductivity must be considered, along with small angle scattering and morphology, which can explain deviations from the theoretical Lorenz number, L. [4, 66] Further, the law assumes that L is a constant, as in the Drude model, but it is actually a material-dependent value, as shown in Table 2. The table also presents L values at 100°C, which shows a consistent increase as compared to 0°C.

Given these drawbacks, researchers have relied on other predictive models, including those based on the Boltzmann transport equation (BTE) to describe the complexity of nanoscale heat transport. [67] The manner by which the electron

distribution function is impacted by a thermal gradient and boundary conditions is described in the BTE.[68]

2.3 Thermal Boundary Resistance (TBR)

As noted previously, heat conduction in nanoscale materials is impacted by interfacial thermal conductivity, which is defined by the ratio of heat flux to temperature drop across the interface of two materials. [10, 67] For thin films, a temperature drop across an interface may be attributed to several factors, including surface roughness, surface hardness, impurities, and contact pressure. An interfacial layer can also exist as a difference in microstructure, bonding, and stoichiometry between the mating surfaces. Given the inherent difficulty in characterizing these differences, the thermal boundary layer can be modeled as a series of anisotropic microvoids located at the interface. Such voids create a change in localized density, thus reducing heat transport through the interface [69]. The interaction between the interfacial properties and thermal boundary conductance (or resistance) results in additional carrier scattering mechanisms. This interaction can impact not only the thermal transport mechanism at the interface, but also control thermal transport throughout the entire nanosystem. Measurement of thermal boundary conductance is often performed at very low temperatures in order to achieve the required measurement sensitivity [15]. Techniques such as Time Domain Thermoreflectance (TDTR) have been used to measure thermal boundary resistance between two solids. This technique is successful due to differences in thermal diffusivity between the interfacial layer and the two mating surfaces. This technique will be discussed further in the next chapter.

The Kapitza length (l_k), or the thickness of the thermal boundary layer, can be

described by the following relationship:

$$l_k = \kappa R_k \tag{8}$$

where κ is the bulk thermal conductivity of the material adjacent to the interface, and R_k is the thermal boundary resistance.[70] In some instances, designers can exploit this relationship by introducing materials at the interface to either promote or restrict thermal transport across boundary layer. Adhesion layers or ion irradiation are two examples of modifying the thermal boundary layer between a thin film and substrate to impact thermal transport. The introduction of adhesion layers in thin film fabrication will be discussed in greater detail later in Chapter 4.

2.4 The Heat Equation

Both electrons and phonons carry heat and contribute to the overall thermal conductivity of materials. Generally, electrons are the primary heat carriers in metals, with some contribution from phonons, while phonons dominate heat transport in dielectrics and semiconductors. Paskov *et al.* investigated the effect of Si doping on the thermal conductivity of GaN and found that increased concentrations of Si doping resulted in a gradual decrease in thermal conductivity, from 240 W/mK for undoped conditions to 210 W/mK for the highest doped sample in the study. [71] The decrease in thermal conductivity was attributed to increased phonon-point defect scattering with higher doping concentrations.

The thermal properties, regardless of the type of heat carrier, are dependent on the specific heat capacity of the carriers, their velocity, and how often they scatter. [56] In the absence of a heat source, temperature evolves according to the heat equation

$$\rho c_p \frac{\partial T}{\partial t} = \kappa \nabla^2 T \tag{9}$$

where ρ is the mass density and c_p is the specific heat capacity of the material. This relationship can also be written

$$\frac{\partial T}{\partial t} = \frac{\kappa}{\rho c_p} \nabla^2 \mathrm{T} = \alpha \nabla^2 \mathrm{T} \tag{10}$$

This leads to the expression for thermal diffusivity α, given as,

$$\alpha = \kappa / \rho c_p \tag{11}$$

As noted previously, for nanoscale materials, heat transport is also a function of the MFP, l, of heat carriers, which is expressed as,

$$l = v\tau \tag{12}$$

where v is the velocity of the carriers and τ is the mean time between scattering events.

Kinetic theory is often used to produce a straightforward connection between mean free path and thermal conductivity, as shown.[72]

$$\kappa = \frac{1}{3} c_v v l = \frac{1}{3} c_v v^2 \tau \tag{13}$$

This relationship can apply to free electrons in conductors since they are generally the main heat carriers in comparison to lattice vibrations (phonons). In this context, it is helpful to consider that the heat flow at a given point is related to the velocity of the carriers and the energy of the carriers following their last scattering event, which is characterized by MFP. The net flow of energy is due to the presence of a temperature gradient.

The application of Fourier law to nanostructures has specific limitations. As Chen [73] observes, heat transfer is a non-equilibrium process, but temperature is an

equilibrium concept. In larger scale materials, deviation from equilibrium is usually small, and local thermal equilibrium can be assumed. However, when the structure is small compared to its MFP, as is the case in nanostructures, thermal equilibrium is not generally established. However, local equilibrium can be established at each scattering event, as stated at the beginning of this chapter, so kinetic theory can be applied. Nanoscale heat transfer is considered to be a ballistic or "quasiballistic" process, as opposed to a purely diffusive process described in Fourier's law.

A dimensionless quantity, the Knudsen (Kn) number, is the ratio of MFP l of the heat carrier to the minimum dimension of a nanostructure, and is used to help delineate various heat transport mechanisms. [74] For example, when Kn<<1, bulk properties prevail, and the heat transfer is diffusive in nature. Conversely, when Kn>>1, the nanoscale heat transport can be considered ballistic, with a quasi-ballistic or diffusion-ballistic regime at intermediate Kn values. This suggests that thermal conductivity is no longer an intrinsic material property but a structural property in the nanoscale. [73]

2.5 Grain Size Effects

An important insight when considering the MFP is the identification of the length scale where the physical dimensions of the material begin to significantly impact the physical properties.[56] Similarly, film thickness and grain size on a similar length scale can dominate heat transport mechanisms. Grain size tends to scale linearly with geometric dimensions (thickness and width) of nanostructures. [75] As film thickness or nanowire widths decrease, the grain size also decreases and the resultant grain boundary area increases due to the growth mode of various deposition techniques.[61] Grain boundaries can be considered either as "coincidence" boundaries with a high level of

symmetry, or “random” with low symmetry.[76] In the case of coincidence boundaries, such as twin boundary, the adjoining grains have several lattice sites in common. When a small angle exists at a coincidence boundary, a step dislocation is formed. Under suitable conditions, a “pile up” of steps can be created which greatly impacts mobility at the boundary. Further, when a stress is applied, the step can generate additional dislocations, thus increasing the overall grain boundary area. Studies conducted by Kim et al. measured a marked difference in copper nanowire resistivity due to grain boundary scattering effects and the degree of structural symmetry of the grain boundaries. [75]

If grain boundaries are immobile, the initial grain size at the base of the film will be very small, but as the film thickness increases, the average in-plane grain size increases, likely due to growth competition at the surface of the film. [77] A columnar structure results consisting of non-equiaxed grains which are related to low grain boundary mobility at the deposition temperature. When materials are deposited at higher temperatures, more equiaxed grain structures form, with a uniform in-plane grain size comparable to the film thickness.[78] Further grain growth can occur during post-deposition annealing. It is important to note, however, that grain growth in thin films experiences highly anisotropic surface and interfacial energy, resulting in preferred growth of grain to minimize these energies. [79] Grain growth can also be impacted by strains imposed by the differential thermal expansion of the substrate relative to the film. Specific crystallographic textures evolve as a result of surface, interface, and strain-energy states, all of which are anisotropic, within the deposited film. [80] These effects can influence thermal conductivity in thin films and nanowires, but are not addressed in the present study.

In this study, the evaporated titanium and gold films grow as islands, commonly described by the Volmer-Weber mechanism. [52] As the deposition thickness increases, the islands coalesce to form a dense, uniform film.

2.6 Summary of Chapter

In this section, the inability to employ classical theory to characterize nanoscale heat transport was discussed. Significant modifications are required to account for the contributions of not only electrons, but phonons and size effects attributed to dimension and grain boundaries. There are specific limitations to the Wiedemann-Franz law for nanoscale materials and the effect of temperature is significant. Finally, the thermal boundary resistance between mating surfaces must be considered. All of these factors must be incorporated to adequately measure and understand nanoscale thermal conductivity.

3. EXPERIMENTAL METHODS FOR THERMAL MEASUREMENT

Many techniques have been explored to measure thermal conductivity on the nanoscale, with varying levels of success. Sample preparation, testing environment control, and parasitic heat losses represent enormous challenges to accurate and reproducible thermal measurements. [81] Prior to introducing techniques for characterizing nanoscale heat transport, it is instructive to review measurements on the bulk scale. In general, thermal measurements fall into two categories: steady state methods and transient methods. [10] In steady-state techniques, the thermal properties of the material are determined by measuring a temperature difference across a prescribed distance that does not change over time. Conversely, transient methods measure time-dependent energy dissipation.

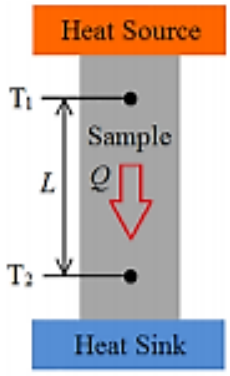


Figure 7. Absolute Temperature Method. [10]

Steady-state measurements, such as the absolute technique shown in Figure 7, are commonly used for bulk materials and involve placing a sample between and heat source and a heat sink with a known power output. The resultant temperature drop across the length between the source and sink is measured. The temperature drop is typically

measured with thermocouples and the thermal conductivity is determined by Fourier's Law, as shown in Eq. 3. Parasitic heat losses due to convection and radiation contribute to the difficulties of such measurements. Performing the test under vacuum can significantly reduce convection and radiation parasitic losses. Additionally, heat lost may be attributed to the apparatus, such as thermocouple wiring, used in the measurement. This technique is limited to larger-size materials, since the diameter of thermocouple wires is on the order of 25 um. Further, this technique requires the determination of the heat flow through the sample. Use of comparative analysis with samples of known thermal conductivity may be useful to determine heat flow.

For materials on the millimeter scale, techniques such as parallel thermal conductance may be appropriate. Similar in nature to the absolute method, the parallel thermal conductance method allows for samples that are too small to support heaters or thermocouples. A sample holder located between a heat source and sink, with a

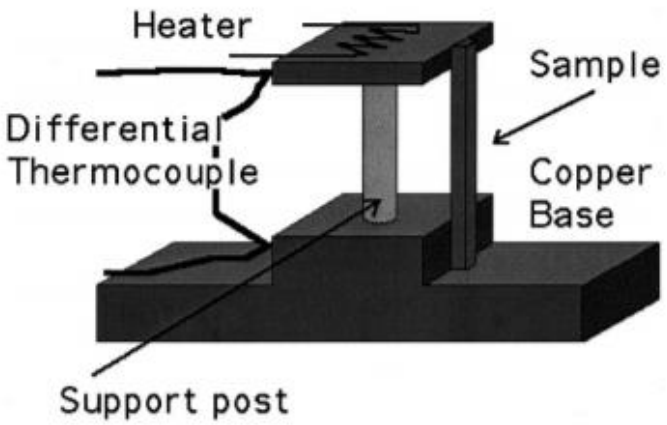


Figure 8. Parallel Thermal Conductance Technique. [9]

differential thermocouple located between the heater and the post on the one junction end, and between the sink and the post on the other junction. Prior to testing, the thermal

conductance of the sample holder must be measured to determine thermal losses from the testing apparatus. Critical to this measurement technique is the accurate determination of the cross-sectional area of the very small samples being measured.

To address the inherent drawbacks of steady-state measurement techniques, several transient techniques have been developed. Unlike the steady-state methods, transient measurements reduce parasitic heat losses, contact resistance of temperature sensors, and the long testing duration required to achieve a steady-state condition. A pulsed power technique introduces a periodic electrical heating current to the sample shown in Figure 9.

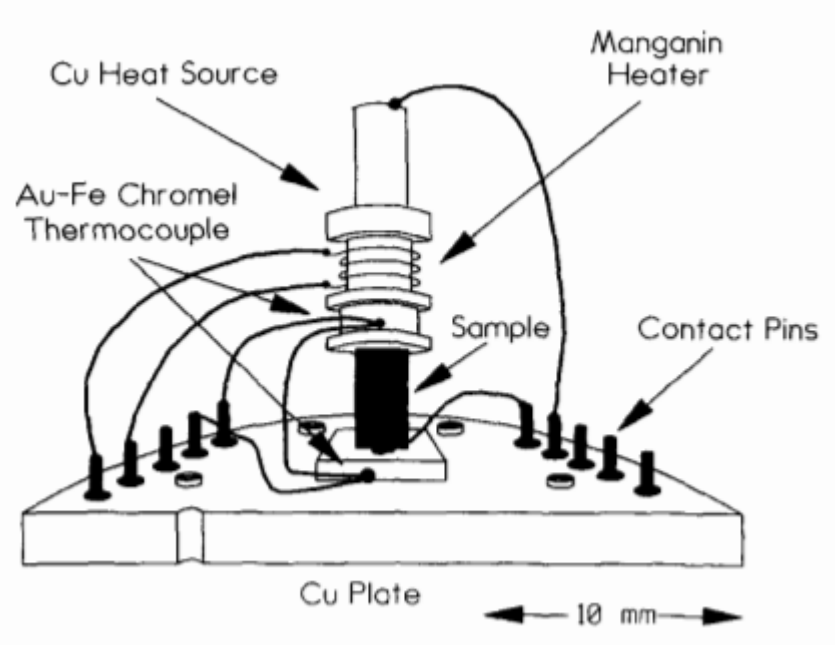


Figure 9. Pulsed Power Technique [7]

Unlike the absolute technique, the heat source current can change during the measurement, either a square wave or sinusoidal, while the heat sink temperature is allowed to slowly drift during measurement. The small temperature gradient between the

heat source and sink is then measured with a thermocouple. The thermal conductance is then measured as a function of temperature. Again, such techniques may be suitable for larger scale samples, but cannot provide the sensitivity and control needed for nanoscale measurements.

The determination of whether a test method is steady-state, quasi-steady-state, or transient is not as clear-cut as it may appear. The spacing between heat source(s) and key material properties help determine the time regime of the experiment to provide context to the measurement. [82] This will be further discussed in Chapter four.

3.1 Optical (non-contact) Methods of Thermal Measurements

Regardless of using a steady state or transient measurement method, contact thermal resistance is a major source of error for temperature measurement. Accordingly, numerous techniques have been developed that employ non-contacting, non-destructive temperature sensing. A laser flash method involves an instantaneous light source used to uniformly heat one side of the sample, while a detector measures the time-dependent temperature rise on the back side. Heat conduction is assumed to be isotropic, with no lateral heat loss. The higher the thermal diffusivity, the faster the heat transfer and resultant temperature rise on the back side.

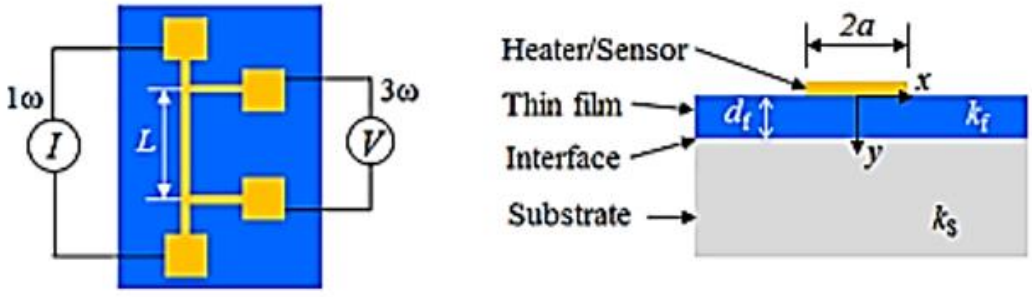


Figure 10. Top and Cross-section View of 3-ω Technique. [10]

The 3ω method is used to measure thermal properties of both bulk materials and thin films, as shown in Figure 10.[67] Developed in 1990, Cahill and his co-workers created a method where a film is deposited on a substrate along with a metallic strip, which serves as both a heater and temperature sensor.[83] A sinusoidal current is applied to the heater/sensor at a frequency ω, which results in a temperature rise proportional to 2ω. There is a third harmonic in voltage drop in the heater/sensor due to the temperature rise.[84] This change in voltage at the 3ω frequency has the information about the thermal transport within the sample. Because this voltage change is very small, a lock-in amplifier is used to obtain a measurement.

There are several key advantages to the 3ω method. Depending on the width of the heater, this technique is useful to measure both cross-plane and in-plane thermal conductivity of thin films. The 3ω method can be used for measuring dielectric, semiconducting, and electrically conducting thin films. One of the main advantages of the 3ω method over steady-state measurements is the effect of radiation heat losses is diminished. Cahill *et al.* determined that the calculated error due to radiation of 3ω measurements is less than 2%.[85] Experiments can be conducted below room temperature using a cryostat, or above room temperature using an evacuated tube furnace.

For electrically conducting and semiconducting materials, the samples need to be electrically isolated from the metallic heater with an additional insulating layer, which introduces a source of thermal resistance and reduces the sensitivity of the measurement. The 3ω method also requires microfabrication, which is time-consuming and costly. For thin films deposited on a substrate, it is important that the thickness of the film is five times the width of the metal strip, which limits the range of film thicknesses that can be

evaluated with this technique. Further, the sample must be smooth and clean in order for the metal strip to sufficiently adhere.

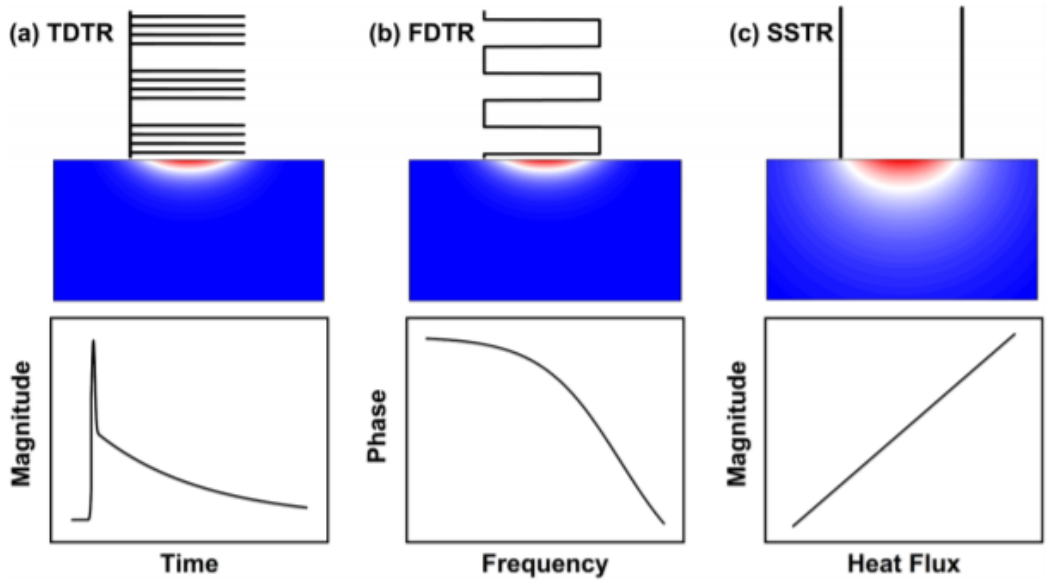


Figure 11. Comparison of Thermoreflectance Measurements [8]

Another non-contact optical heating and sensing method for measuring thermal properties is transient thermoreflectance (TTR). The technique can be implemented as either time-domain (TDTR) or frequency-domain (FDTR). Both bulk and thin films can be measured using this technique, where a thin metal film (typically aluminum or tungsten) is deposited on the sample to serve as a transducer layer. The reflectance of the transducer layer changes with temperature at the laser wavelength and is measured as a thermal response. In TDTR, the thermoreflectance is measured as a function of the time delay between the arrival of the probe and the pump pulses on the sample surface. In recent years, this technique has been used for measuring anisotropic thermal conductivity of thin films and for probing spectral phonon transport. The thermoreflectance change is extracted using a photodiode and a lock-in amplifier.

In FDTR, changes in thermoreflectance are measured as a function of the modulation frequency of the pump beam. The advantage of FDTR is that the probe delay is fixed so any error associated with the mechanical stage is eliminated.

The third method shown in Figure 11 is Steady State Thermoreflectance (SSTR), where the thermoreflectance is measured with increasing pump power in a lower modulating frequency as compared to TDTR and FDTR. By comparison, this lower frequency results in a greater penetration depth, as illustrated in Figure 11.[8]

Additional non-contacting methods such as infrared thermography, Raman spectroscopy, optical interferometry [86], and fluorescence thermography have all been investigated as means of evaluating thermal effects and properties.[87] Unfortunately, these techniques are diffraction limited and achieve spatial resolution on the order of a few hundred nanometers to microns, which is not sufficient for nanoscale measurements. [88] Moreover, each approach is applicable for specific material systems, as is the case for Raman spectroscopy which is suitable only non-metallic materials.

3.2 Contact Methods of Thermal Measurement

Contact measurements have also been explored to characterize both cross-plane and in-plane thermal conductivity of thin films. In this process, a thin film is grown or deposited on a flat surface, such as polished silicon. A metallic strip is then deposited on the thin film and a direct current is passed through the strip. The advantage of techniques based on resistive thermometry is that they provide a direct measurement of the temperature rise and can be related to thermal conductivity of the sample through precise knowledge of the sample geometry and the electrical resistivity reference.[15] The technique used in this study is a variant of this method and will be discussed at length in

the next chapter.

Several studies of nanoscale thermal properties involve the fabrication of suspended structures and/or wires in order to thermally isolate the sample by preventing parasitic losses into the substrate. The suspended wire geometry eliminates the thermal boundary layer imposed by the presence of a substrate. Suspended wire studies involve the fabrication of the wires on a sacrificial substrate, with a subsequent etching process to create a trench, thus suspending the wires. This is an exceedingly difficult task, with the potential for changing the topography of the wire or introducing defects from the etching/removal process.

Another contact approach that shows promise involves the use of nanomanipulators *in-situ* in a scanning electron microscope. [89] In this study, researchers employed nichrome nanoprobes/nanotips to interrogate individual nanowires. These specialized tips were created to address the inherent difficulty involved in obtaining reproducible Ohmic contacts on nanopatterned materials. Poor ohmic contact creates significant scatter in measured properties. Additionally, tungsten is often used as a tip material which easily oxidizes over time, potentially impacting the contact characteristics of the probe. Further discussion of ohmic contacts and probe tip integrity is discussed in a later section.

Recent advances in scanning thermal microscopy (SThM) have shown the capability of achieving spatial resolution down to 10nm, making it an attractive option for thermal measurements, imaging, and the study of thermal transport phenomena in nanosystems.[90] SThM is a derivative of atomic force microscopy (AFM) that employs a temperature-sensitive probe which contacts the surface of a sample. When the probe tip

contacts the sample and is raster-scanned across the surface, heat flows between the tip and sample, and a thermal map is generated by a measured thermal signal. Using this technique, SThM can distinguish between different types of materials based on their thermal conductivity due to the relative amount of cooling of the probe tip during contact. [91] Due to excellent thermal and spatial resolution, SThM can provide a qualitative assessment of thermal conductivity within a sample. [88]

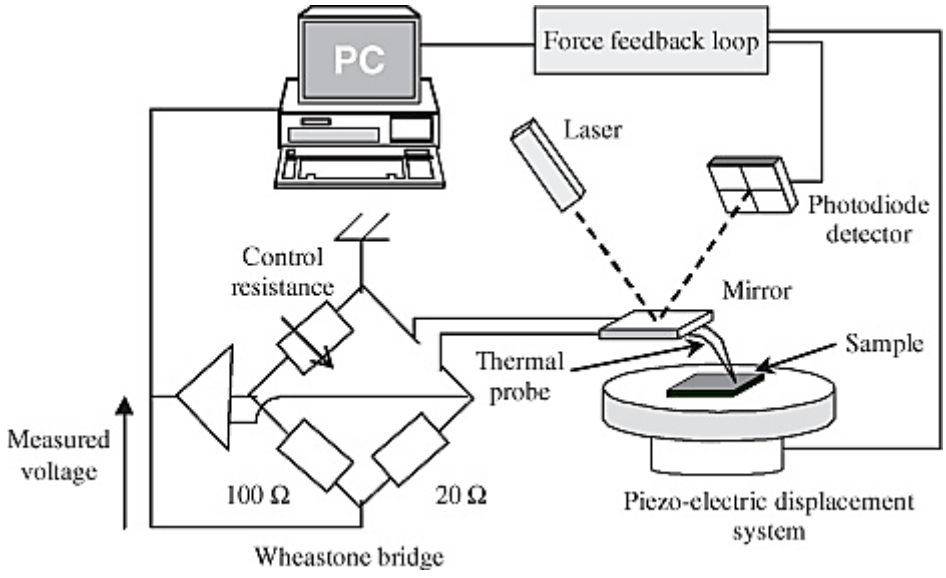


Figure 12. Scanning Thermal Microscopy (SThM) Experimental Set-up [2]

SThM systems can operate in either the passive or active mode. In the passive mode, the sample is heated and contacting probe measures the resultant thermal signal. In the active mode, the probe is heated by an applied current, resulting in localized heating of the sample. In either mode, a flux-creating signal is measured. The challenge of this technique is relating the measured signal to a property of interest.

In order to relate the measurement to a value of thermal conductivity, it is important to understand the physical characteristics of the measurement itself. Figure 12

illustrates a typical SThM measurement system.

Similar to a standard AFM, a sample is placed on a piezo-electric stage and is contacted by a very sharp probe connected to a cantilever. There are numerous probes commercially available for SThM measurement systems, including thermoresistive and thermocouple probes that are capable of measuring the thermal interaction at the interface between the probe tip and the sample surface. Depending on the type of probe, this thermal interaction is measured as a resistance change, a Seebeck coefficient, or a bimetal effect. Commonly used probes include Wollaston (Pt) wires, doped Si resistive, and PD coated Si_xN_x configurations.[88] The probes have a tip apex on the order of a few nanometers, which provides the high level of spatial resolution. A laser and photodiode detector are positioned above the probe-cantilever assembly in order to measure displacement. The thermal probe is connected to one arm of the Wheatstone bridge circuit, in addition to two resistors of known value and a variable resistor used to balance the bridge. At the beginning of the measurement, the circuit is balanced by adjusting the "reference" resistance to match the probe resistance using the variable resistor. During the actual measurement, the resistance of the probe changes in response to localized heating at the tip sample interface, either by the heated sample (passive mode) or by Joule heating by an applied probe current (active mode). The measured thermal signal is from the tip-surface interaction is very small, so the signal is amplified.

Using this technique, the SThM method can distinguish different types of materials based on their thermal conductivity due to the relative amount of cooling the probe tip experiences at contact. [91] Materials with high thermal conductivity will produce a relatively small thermal signal, because the heat is efficiently removed from

the tip-sample interface. Conversely, lower thermal conductivity materials will produce a higher thermal signal, because more heat remains at the tip-sample interface. Due to excellent thermal and spatial resolution, SThM promises an excellent qualitative assessment of thermal conductivity differences within a sample.

A significant challenge to performing measurements of this nature is understanding and characterizing the impact of various heat transfer mechanisms in the system. One approach by Gomes *et al.* considers various heat transfer channels that exist between the probe and the sample.

An initial approach of this study was to correlate the measured thermal signal from the probe to a thermal property of the sample. Various calibration techniques were explored, including the use single crystal bulk samples of known thermal conductivity, to establish a quantified measurement system. Unfortunately, difficulties arose when trying to correlate the thermal signal from the device to a sample of known thermal conductivity. Numerous equipment difficulties were encountered, resulting in long repair delays. It was determined that further SThM work could not reasonably continue within the time-constraints of this project.

3.3 Summary of Chapter

In this chapter, a selection of techniques for measuring thermal conductivity of bulk and nanoscale materials were reviewed. It is clear that testing methodology has experienced a remarkable evolution over the past fifty years. Different testing environments and improved spatial resolution have served to expand the knowledge base of thermal behavior for a vast array of material systems. However, the ability to conduct these tests in a timely, reproducible fashion is often lacking. Extensive sample

preparation and calibration methods can minimize the effectiveness of the measurement.

In the next chapter, a microelectrothermal testing technique to measure the thermal response of nanoscale materials is discussed, which allows a direct measurement of thermal conductivity.

4. THERMAL CONDUCTIVITY MEASUREMENT OF NANOWIRES

As mentioned in the previous chapter, researchers have explored both contact and non-contact methods to measure the thermal properties of materials. [10, 59, 67, 86-93] The challenge of either method arises when measuring materials on the nanoscale. Often, the size of the energy source, whether an optical "spot" or a contacting probe, exceeds the dimension of the material under consideration. In this study, a novel contact method of measurement is used, which allows for direct measurement with minimal influence of the testing equipment.

4.1 Microelectrothermal Testing

Stojanovic *et al.* conducted direct measurements of electrical and thermal conductivities of rectangular aluminum nanowires of varying widths using a microelectrothermal test structure, similar to that shown in Figure 13 from the current work [47, 49, 50]. This dissertation leverages that prior work.

The test structure consists of a resistive heater situated between two resistance temperature detectors (RTD) that are separated by 1 μm. The inset in the figure is a magnified view of the central portion of the test structure, where the nanowire array of 33 μm length is positioned in a comb-style fashion along the length of the sample trace. The test structure, inclusive of the nanowire array, consists of evaporated gold supported on a silicon dioxide/silicon substrate. As is the case in the Stojanovic et al. studies, the device used in this study is analogous to an electric bridge circuit, except the thermal response is characterized as opposed to electrical impedance. An electric drive current is applied to the contact pads of the heater resulting in Joule heating. Simultaneously, the resistance

change across the two contact pads of the sample and reference RTDs is measured.

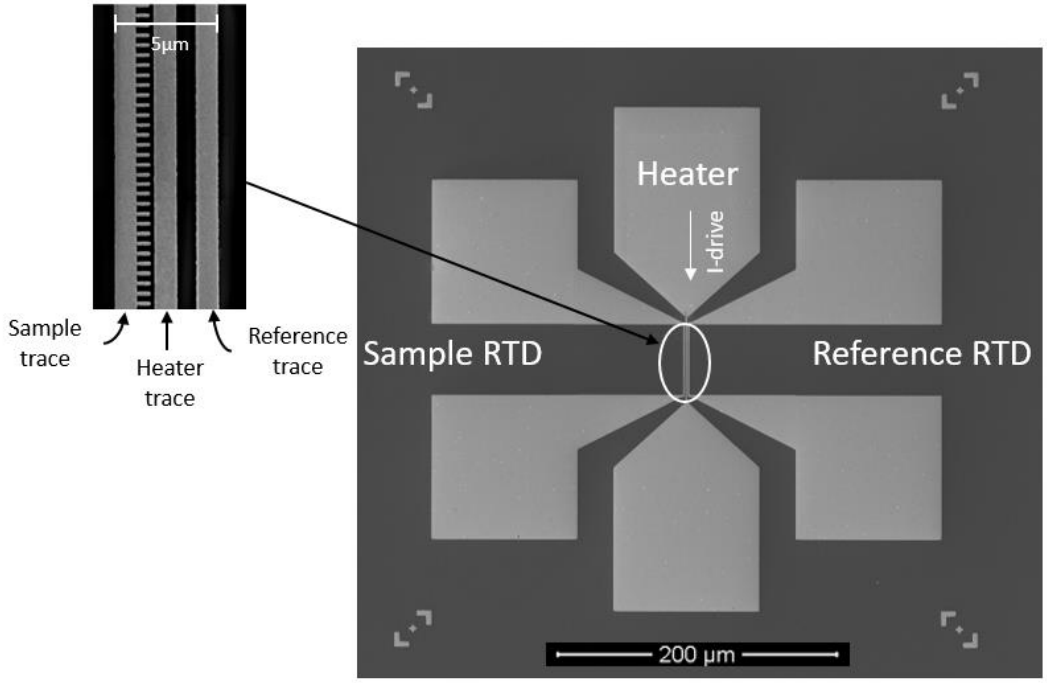


Figure 13. Microelectrothermal Test Device.

The presence of the nanostructure array on the sample RTD, as shown in Figure 13, breaks the symmetry of the device, causing an imbalance in temperatures between the sample RTD and the reference RTD. Consistent with the Stojanovic *et al.* studies, the mode of heat transfer is assumed to be primarily conduction through the substrate, with negligible effects of radiation and convection modes. The thermal conductance of the nanostructure array can be estimated by calculating the temperature difference from the resistance imbalance measured by the RTDs imposed by the drive current through the heater. As noted in the Stojanovic work, parasitic losses into the substrate will still exist, but they will be an equivalent effect on both the sample and reference RTDs.

4.2 Selection of Substrate Material

While the Stojanovic *et al.* study used a glass wafer substrate, due to the low thermal conductivity of SiO_2, the present study used silicon wafer coupons with a thermally-grown 2 μm oxide layer as the substrate material. The silicon dioxide/silicon substrate affords several key advantages. First, the roughness of the oxide layer is quite low (0.2-0.3 nm RMS), thus reducing the inherent thermal boundary resistance between the nanostructure as compared to ~1.5 nm RMS for glass wafers.[94] Further, the silicon dioxide/silicon substrate allows flexibility to evaluate post-processing treatments such as annealing, while elevated temperatures can result in cracking and delamination with glass substrates. Finally, the Si/SiO_2 wafer coupon is somewhat easier to pattern via e-beam lithography as compared to the glass wafer due to substrate charging. This effect will be discussed in Section 4.3.

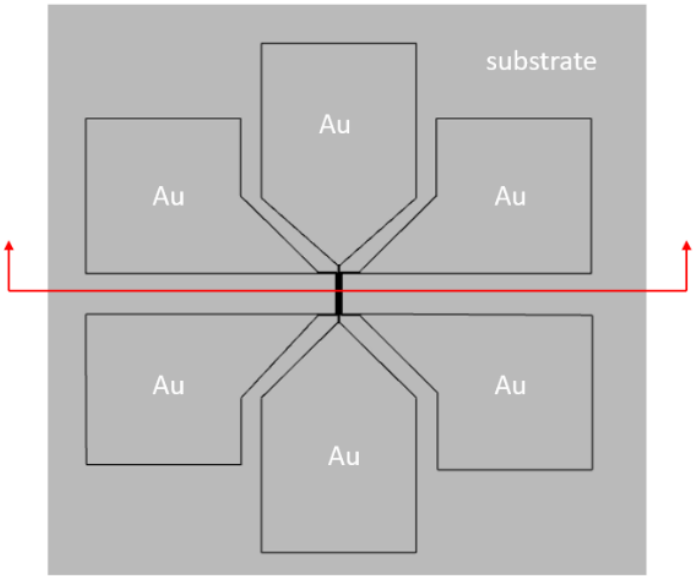


Figure 14. Model Geometry of Microelectrothermal Device with Cut-plane.

To ensure suitable thermal isolation could be achieved, COMSOL® Multiphysics simulations were conducted prior to experimentation to compare the extent of thermal isolation of glass and silicon dioxide/silicon substrates. Both the heat transfer and the electric circuit modules were used in the model to simulate the thermal response of the sample and reference sensors with a current source to the heater. COMSOL® modeling is a finite element analysis (FEA) program that will be discussed further in Chapter 5.

The model geometry, as shown in Figure 14, illustrates the use of a cut-plane to evaluate a cross-section of the device (cut-plane shown as the red line traversing the structure). Key material properties and model parameters used in the simulation are shown in Table 3. Most of the parameters are identical, with a key difference in the thermal conductivity between the silicon dioxide and glass. The bulk thermal conductivity value for gold was used in the simulations, given the relatively large dimensions of the heater and RTDs traces (1 µm width). The room temperature simulation results for the SiO_2/Si substrate are shown in Figure 15. The simulation indicates that the heater achieves a maximum temperature of 360K at a 25 mA drive

Table 3. Material Parameters for FEA Simulations

Key Parameters for Simulation	**SiO_2/Si substrate**	**Glass wafer substrate**
Thermal Conductivity of Substrate [W/mK]	1.4 (2µm SiO_2 layer)	1.13
Thermal Conductivity of Gold device [W/mK]	317	317
Heat Capacity [J/kgK]	730	754
Density [kg/m^3]	2200	2230
Drive Current [mA]	0-25	0-25
Ambient Temperature [K]	298	298

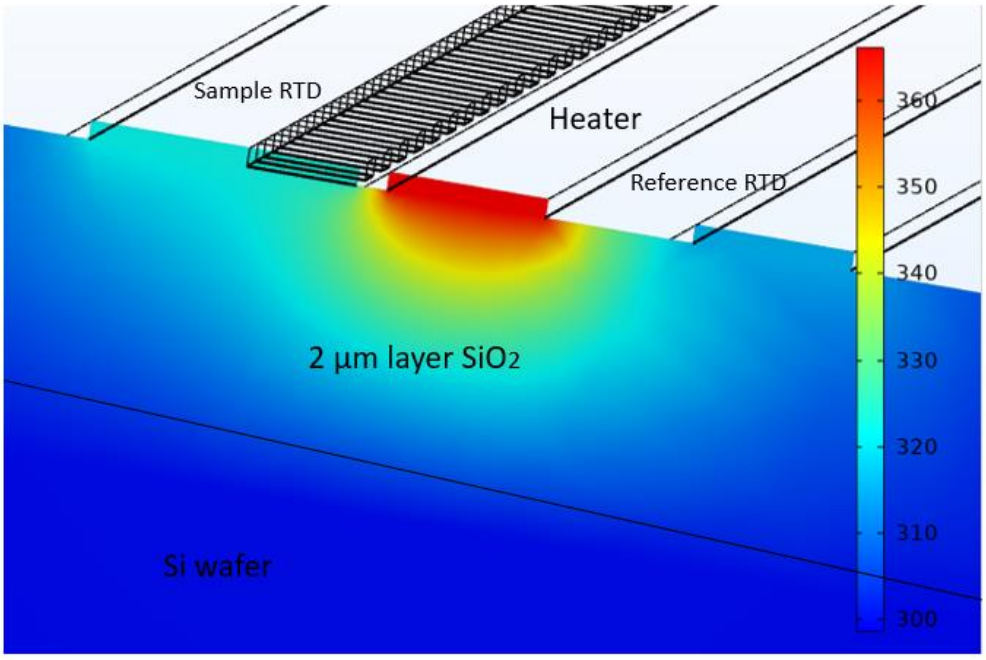


Figure 15. FEA Simulation Results with a Cut-plane for a SiO2/Si Substrate.

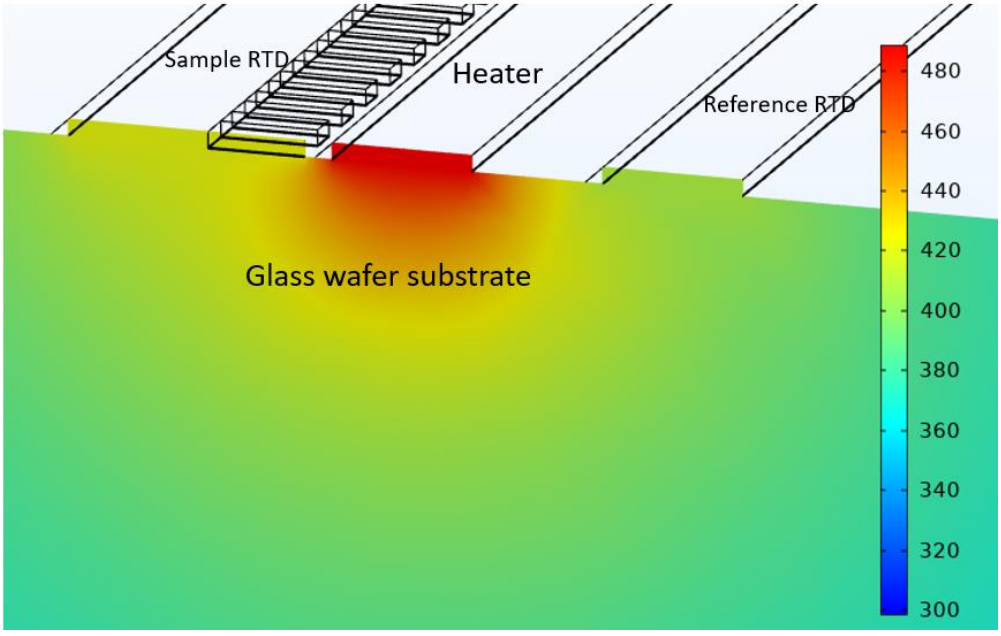


Figure 16. FEA Simulation Results with a Cut-plane for a Glass Wafer Substrate.

current. The cut-plane provides insight on the predicted heat flow resulting from the drive current. The thermal energy is shown to penetrate into the substrate, and reaches ambient temperature at approximately 2 μm depth, which is the thickness of the oxide layer. The temperature difference between the sample RTD and the reference RTD is evident, where the presence of the 230 nm wide nanowire array promotes increased heat flow to the sample RTD, resulting in an increased temperature as compared to the reference RTD.

The FEA simulation results for the glass wafer substrate at room temperature is shown in Figure 16. The temperatures generated from the 25 mA current sweep are significantly greater than those seen in the SiO_2/Si substrate simulation. The simulations confirmed that the glass substrate does indeed provide greater thermal isolation as compared to the silicon dioxide/silicon. Due to the lower thermal conductivity of the glass wafer substrate as compared to SiO_2, the heat generated from the drive current is not dissipated into the substrate. At a 2 μm depth into the glass substrate, the temperature is estimated to be 407K, 100K greater than the SiO_2/Si substrate. If the glass substrate had the same thermal conductivity as SiO_2, the temperature at 2μm depth into the substrate is estimated to be 386K, suggesting that the Si substrate plays a significant role in the dissipating the heat. Ambient temperature is not reached in the glass substrate until the bottom surface of the glass wafer. Decreasing the maximum drive current to 15 mA on the glass wafer substrate yields a similar temperature profile to that seen with the Si/SiO_2 substrate.

Ultimately, the goal in selecting a suitable substrate material is to achieve a significant, measurable difference between the sample and reference RTDs. In the case of the 2 μm thick SiO2 on Si substrate simulation shown in Figure 15, the temperature

difference between the sample and reference RTDs is 7K, while the temperature difference is 13K for the glass wafer for a current sweep to 25 mA with a 230 nm wide nanowire array geometry at room temperature, shown in Figure 16. These temperature differences, as calculated by the measured voltage change in each RTD, can be readily detected by the testing system. For the advantages discussed previously and the ability to measure temperature differences in the two RTD sensors, the SiO_2/Si substrate was selected for this study.

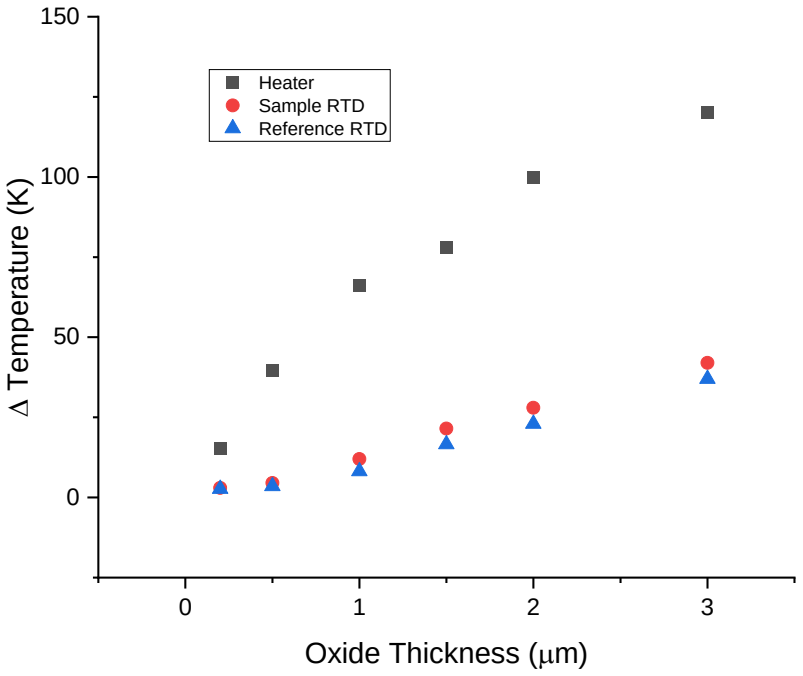


Figure 17. Effect of Oxide Thickness on Temperature Rise of Heater and RTDs. at Room Temperature

The effect of oxide thickness on device temperature is illustrated in Figure 17. A series of FEA simulations was performed to determine the optimal thickness of the oxide layer to achieve a measurable temperature difference between the two RTDs for a 25 mA current sweep at room temperature. As expected, the temperature rise increases with

increasing oxide thickness due to the improved thermal insulation provided by thicker oxide layers. Typically, the native oxide layer on a silicon wafer is 2-3 nm thick and commercially-available grown oxide layers are often in the 200-500nm range. As evident in the Figure 17, a 500nm layer is not sufficient to provide thermal isolation of the device because the difference in sample and reference RTD temperatures is not significant. Therefore, larger oxide thicknesses are warranted, either through a time-consuming process of in-house oxide growth or through commercial means.

Fortunately, 2 μm-thick oxide, 100 mm diameter <100> wafers were available from UniversityWafer, Inc. (Boston, MA), which were diced via laser cutting to achieve uniform 1.5 cm coupons. This same supply of wafer coupons was used to fabricate all the devices used throughout the study.

4.3 Patterning of Test Devices

Over the course of this research effort, over 90 wafer coupons were processed to develop and refine the fabrication methods and testing procedures. Initially, the test structures were going to be fabricated using a combination of photolithography for the contact pads and traces, and e-beam lithography (EBL) for the nanostructure arrays. Conventional photolithography techniques have resolution restrictions due to the diffraction limit imposed by the wavelength of the UV light source, potential mask defects, and the resolving capability of the photoresist [95]. After several attempts at combining the two methods, it was determined that exclusive use of EBL to pattern the entire test structure afforded the best fidelity of the structures, despite the considerable time required for generating the patterns. EBL is a maskless method that employs an electron beam as a means for exposing the desired pattern. An added benefit of an all-

EBL process is the ability to alter the pattern by modifying the design software, as opposed to generating new photomasks in a traditional lithography process.

Preparation of the wafer coupon took place in a cleanroom environment. Initially, the wafer pieces were cleaned using an ultrasonic bath with the following conditions: 5 min. acetone, 5 min. methanol, 5 min. isopropyl alcohol, followed by a nitrogen blow-dry and a 1 min. bake at 180°C. After cooling, the wafer piece was placed on a small adapter inside a Laurel spin-coater.

Polymethyl methacrylate (PMMA, Kayaku Advanced Materials, formerly MicroChem, Westborough, MA) is a commonly used positive resist for e-beam lithography. PMMA is available in several different formulations, with varying molecular weights (MW) and carrier solvents. In this study, both 495K MW PMMA and 950K MW PMMA in anisole (A4) were evaluated, with and without the addition of a MMA co-polymer (methyl methacrylate) layer. Depending on the design of the pattern, a co-polymer can be helpful to generate an undercut in the developed pattern, allowing for improved lift-off. With the test structure design in this study, it was found that a single layer of the higher molecular weight 950K PMMA A4 was sufficient to generate the desired pattern with sidewall integrity.

A Finnpipette was used to statically dispense 200-250 µL of resist on the wafer coupon. The spin conditions were 4000 rpm (with an acceleration of 1200 rpm/s) for 45 s. The resist application was followed by a softbake on a Brewer bakeplate set to 180°C for 90 s. The thickness of the PMMA layer was approximately 200 nm as determined by optical reflectance (Filmetrics San Diego, CA). Variability in resist thickness can greatly impact the ability to generated consistent, repeatable dimensions of

the test device and nanostructure array.

Although PMMA has low UV-sensitivity, care was taken to pattern the wafer coupon in the SEM as soon as possible after the resist was applied to minimize resist exposure. The coated wafer coupon was transferred outside the cleanroom in a closed container to a laboratory containing the Field Emission Scanning Electron Microscope (FE SEM - FEI Helios Nanolab 400 Dual Beam, Thermo Fisher Scientific, Hillsboro, OR). The coupon was affixed to a SEM stub with a Faraday cup, in order to confirm the beam current in the SEM using a picoammeter (Keithley Model 6485).

While it was experimentally observed that the Si/SiO_2 does not charge as much as a glass substrate, as discussed in Section 4.2, care must be taken to minimize charging effects. [96] Charging occurs when the incident electrons from the SEM arrive at an insulating surface and become trapped due to the lack of a grounding path. [97] The built-up charge in the sample causes image distortion and, in the case of e-beam lithography, pattern irregularities. Several techniques are available to minimize the effect of charging on insulating samples, including the application of a thin metallic layer on the surface of the sample, while establishing a current shunt to the SEM chuck, or use of a lower beam energy[98]. However, both of these techniques have limitations. Use of a conductive metallic layer has been shown to be effective, but requires the additional step of metal layer removed via etching prior to developing the pattern. Adjusting the beam energy, particularly in e-beam lithography, is not always practical. While lowering the beam energy via accelerating voltage can effectively reduce specimen charging, it also reduces the penetration depth of the electrons into the PMMA and results in a broadening of the beam spot. [99] In this study, it was found that copper tape provides an adequate

conductive path from the sample coupon to the aluminum stub and shuttle to reduce charging effects without the application of a metallic surface layer.

Each test structure pattern was created using a computer-aided design program (DesignCAD). Nabity Pattern Generation System (NPGS, JC Nabity Lithography Systems, Bozeman, MT) was used to interface with the SEM in order to expose the wafer coupon with the desired pattern(s) dictated by the CAD file. [100] Automated SEM stage movements facilitated the creation of multiple test structures on a given coupon.

The schematic shown in Figure 18 details the SEM stage movement during the patterning of twelve devices, represented by the black boxes on the grey wafer coupon. Prior to patterning, a diamond scribe is used to create a small scratch at the bottom of the coupon. At the end of the scratch, marked by "X" in the schematic, the focus and stigmation are adjusted at the maximum magnification of 2000x. The focus and stigmation are critical to achieving the desired dimensions of the test device and nanostructures. After a sharp, clear image of the scratched area is achieved, the beam

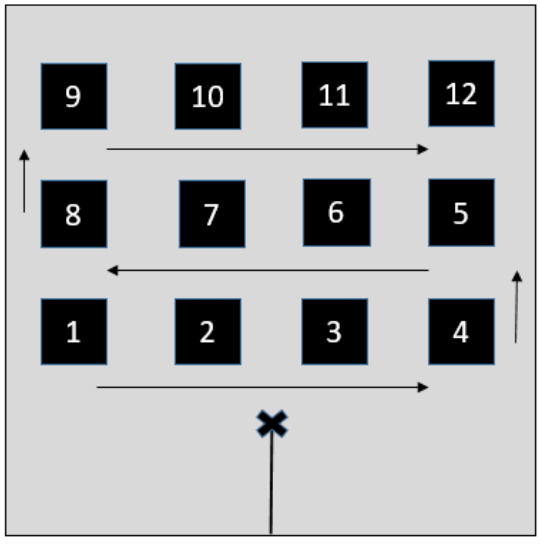


Figure 18. Configuration of Test Devices on Wafer Coupon for EBL.

blanker is activated, and the Nabity runfile is initiated. The run file directs the stage to move from the scratch to the location of device #1 and then directs the beam to expose the surface as prescribed by the DesignCAD file. While the SEM stage is capable of moving 100 mm in the x- and y-directions, the maximum writing field for the SEM is 500 µm x 500 µm. Each test structure requires a writing field of 480 µm x 480 µm for the 2000x magnification required to pattern the smallest features.

Electron beam exposure serves to break the bonds of the large PMMA molecular chains, leaving smaller chains that are soluble in the developer. Once the pattern is complete, the stage moves to the next device as shown by the arrows on the schematic.

The beam current, as measured in the Faraday cup prior to the EBL session, was inputted into the Nabity software to establish exposure dosage. A series of experiments were conducted separately to determine the appropriate dosage for each geometry.

Following exposure, the wafer coupon was developed using a 3:1 methyl isobutyl ketone (MIBK, Sigma-Aldrich, St. Louis, MO) to isopropyl alcohol (IPA) mixture. The coupon was swirled in the mixture for 60 s, followed by immersion in IPA only for 60 s and a nitrogen blow dry.

Several key changes were made to the original design and fabrication process pioneered by Stojanovic *et al*.[47, 49, 50] In the previous study, the heater and RTDs were patterned and metallized first, and then a secondary e-beam lithography process was performed to pattern the nanowire arrays with subsequent metallization. A thin film of chromium and gold was deposited for the heater and RTDs, while aluminum was deposited for the nanowire arrays.

In the present study, the heater, RTDs, and nanostructure arrays were patterned

and metallized as part of a single process. During the e-beam lithography process, one CAD file was created with 2 distinct layers: one layer for the heater and RTDs and a second layer for the nanostructure array. Due to the relatively large size of the contact pads (120 µm square) and heater traces (1µm width), the first layer was patterned at magnification of 150x, 340 pA beam current, 30kV accelerating voltage, and 3 nC/cm line dosage. Once completed, the SEM magnification was increased to 2000x to pattern the second layer containing the nanostructure array, with the same beam settings as the first layer and the line dosage varying from 1 – 1.3 nC/cm, depending on the width of the nanostructures. The filled polygons of the contact pads and traces of the heaters and RTDs were patterned with a serpentine mode where the beam passes back and forth to fill the area. For the narrow (<200 nm width) nanowire arrays, the "one-sided fill" mode was employed, where the writing was initiated from one side only for each line. The one-sided fill appears to provide better resolution for fine features in the design as compared to the serpentine beam motion. Similar to resist thickness, variability of e-beam current and SEM stage alignment impacts the ability to generate consistent, repeatable dimensions of the test device and nanostructure array.

The CAD design of the test structures was adjusted to accommodate the inherent shift in the image area which occurs when the microscope magnification has changed. This approach remedies a significant challenge of the previous study, specifically the alignment of the nanowire array between the heater and sample RTD in the test structure. By patterning the heater, RTDs, and nanostructure array in a single e-beam lithography runfile, the ability to position the array is greatly improved due to variations in stage alignment and coupon orientation.

It is important to note that the current approach requires that the heater, RTDs, and the nanostructure array all consist of the same material, as opposed to one material for the heater and RTDs and a different material for the nanostructure array. By fabricating the entire test structure and nanostructure array with the same material, the thermal boundary layer between nanowires and the sensor trace is eliminated, along with potential thermal expansion differences between the sample RTD and array materials.

4.4 Metallization and Lift-off of Test Devices

The newly-patterned coupon was then returned to the cleanroom for metallization via physical vapor deposition (PVD) and lift-off. E-beam evaporation was the selected for metallization for its capability to generate uniform films with low impurity levels, critical for nanoscale studies. The study coupons were metallized in the Angstrom Engineering EvoVAC E-beam Evaporator (Kitchener, ON Canada). The coupon was loaded into the main chamber of the evaporator with a vacuum setting of 3.6×10^{-8} torr and a throw distance of 47 mm. A 5 nm adhesion layer of titanium was first deposited at a rate of 0.5 Å/s using a spiral source. Without breaking vacuum, a second layer of Au (source purity 99.9999%) was deposited atop the titanium layer, with an initial deposition rate of 0.5 Å/s, increasing to 3 Å/s using a spiral source. Two deposition thicknesses were used in this study: 50 nm and 100 nm. Layer thickness values were controlled by Quartz Crystal Monitors (QCM) inside the evaporator chamber and confirmed by SEM measurements. All depositions were conducted at nominal sample holder temperature of 25°C, and all evaporation materials were sourced from Kurt J. Lesker Company (Jefferson Hills, PA).

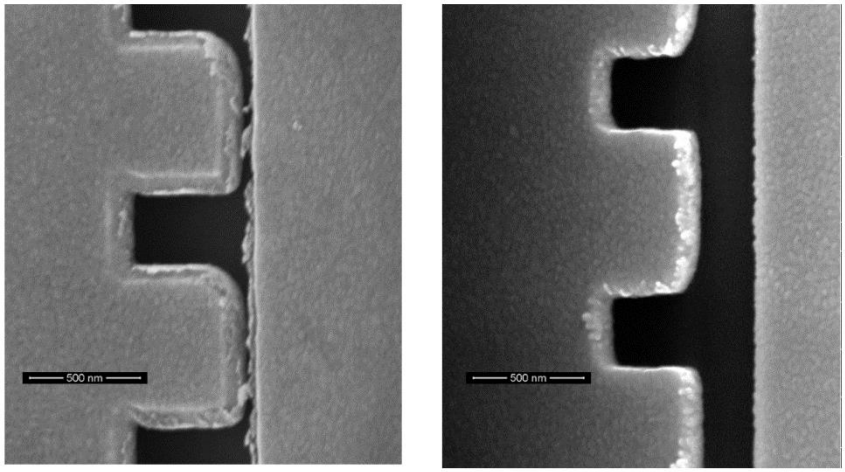


Figure 19. Lift-off Comparison at 45° Tilt.
(overnight soak in acetone (left) and 5 min sonication in acetone (right))

After metallization, a lift-off process was performed. It is critical during the lift-off process that the test device is completely free of any residual metals. Several techniques were evaluated to achieve complete lift-off without damaging or removing the fine nanostructures. Two different lift-off techniques used on nanofilm arrays are shown in Figure 19. Both SEM images were captured at 50,000x magnification at a 45° tilt. The array to the left was soaked in acetone overnight, followed by an IPA rinse and N_2 blow dry. Incomplete lift-off is evident in this image, with residual material residing in the gap between the RTD and heater. The residual material affects the final dimensions of the nanostructures and interferes with the desired electrical isolation between the heater and the RTDs. Interestingly, subsequent sonication treatments were not successful in removing this residual material. The array shown on the right was sonicated for 5 min in acetone immediately following metallization, followed by a 1 min sonication in IPA and a N_2 blow dry. The sonication method resulted in a clear gap between the heater and RTDs and sharper edges of the nanostructures as compared to the soaking method.

Sonication was used for the fabrication of all test devices in this study.

4.5 Nanostructure Geometries

Different nanostructure array configurations were considered in the study to optimize the resultant temperature difference between the sample RTD and reference RTD for a given drive current. In the Stojanovic *et al.* study, the nanowire arrays were

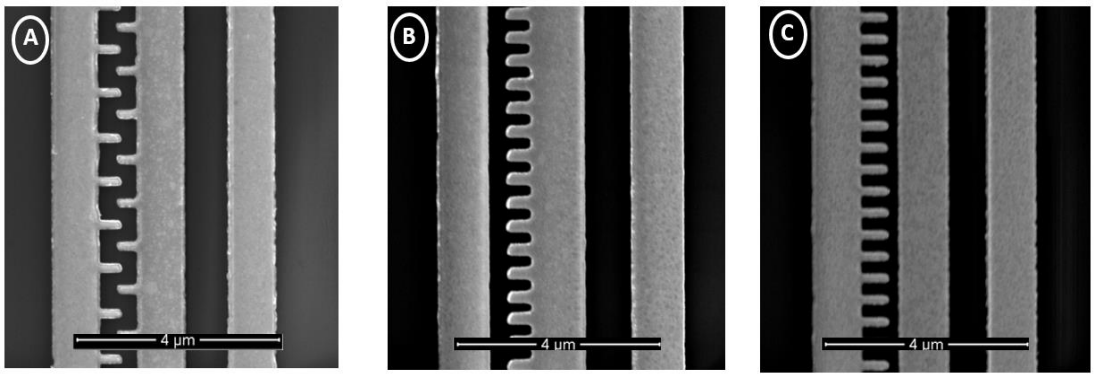


Figure 20. Nanowire Array Configurations.
(A) Interdigitated, (B) Comb H to S, (C) Comb S to H

fabricated in an interdigitated fashion. These were also fabricated as part of the study as shown in image A of Figure 20. Additionally, two alternate configurations were also evaluated as shown in Figure 20. Image B represents the nanostructure array extending from the heater toward the sample RTD (designated as “comb H to S”), while image C illustrates the nanowire array extending from the sample RTD toward the heater (designated as comb “S to H”). Samples with the three different configurations were generated for both nanowire and nanofilm arrays.

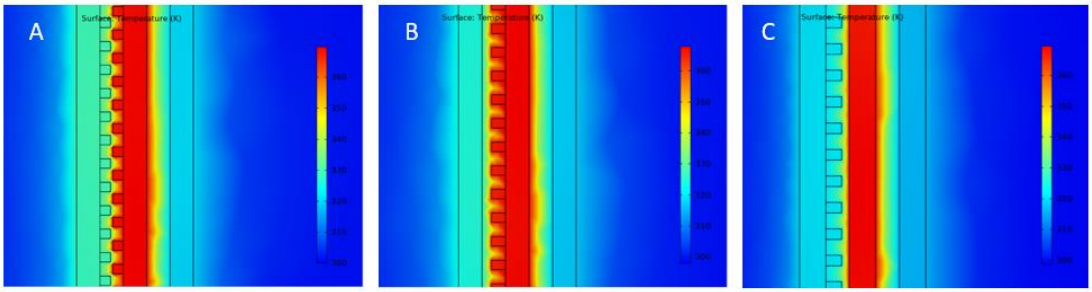


Figure 21. COMSOL® FEA Simulation Results of 3 Nanostructure Configurations.
(A) interdigitated, (B) comb H to S (C) comb S to H

The thermal FEA simulation of the three configurations with nanofilm arrays are shown in Figure 21. This comparison provides insight regarding the heat transfer process between the heater and the two RTDs. The images indicate a difference in the temperature distribution across the heater and two RTDs based on the nanowire array configuration.

The experimental results from electrical testing for the three nanofilm configurations is shown in Figure 22, Figure 23 and Figure 24 along with its corresponding SEM image. Each test was performed at 300K temperature with a heater current sweep of 0 to 25 mA. The film data is presented instead of the nanowire devices shown in Figure 20 for two important reasons. First, all the devices with film arrays were fabricated at the same time with identical geometries, so it can be assumed that the thickness of the metal deposition and the material properties are identical for all three devices. Secondly, electrical probe testing of the devices is a destructive process and there is a limited number of times that a given device can be interrogated before it is on rendered unusable. In the case of the devices with nanowire arrays, fabrication took place different days and one of set of devices was destroyed during electrical testing.

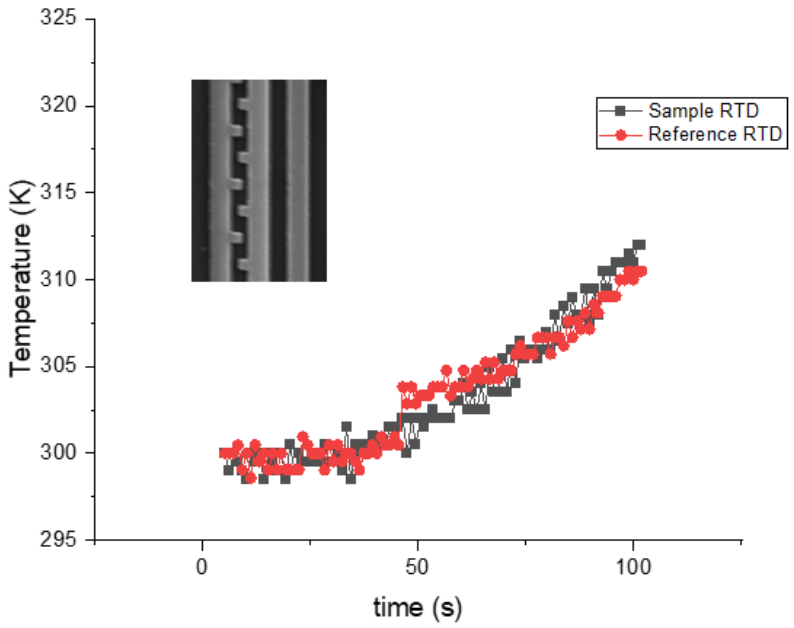


Figure 22. Thermal Response of Device with Interdigitated Nanofilm.
25 mA, I-V sweep at 300K

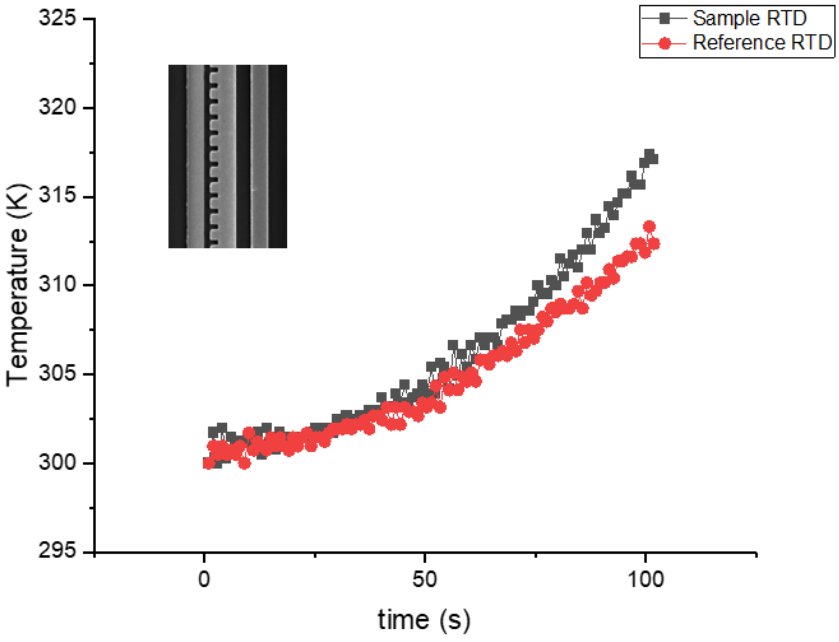


Figure 23. Thermal Response of Device Nanofilm (Comb H to S).
25 mA I-V sweep at 300K

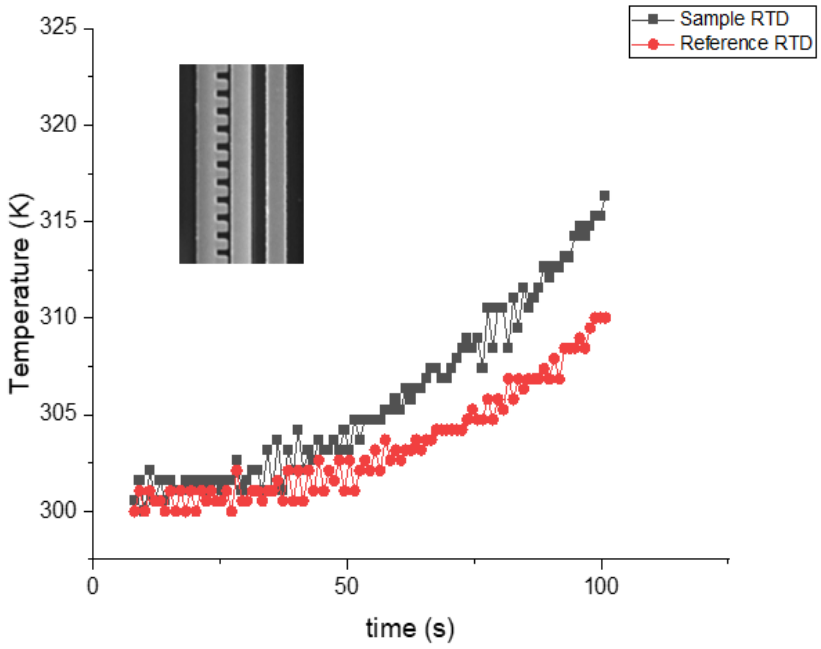


Figure 24. Thermal response of device with nanofilm array (Comb S to H).
25 mA I-V sweep at 300K

The experimental results demonstrate that the different array configurations play a significant role in generating a temperature difference between the sample RTD and reference RTD. The interdigitated condition, shown in Figure 22, produced a very small temperature difference between the two RTDs, while both Figure 23 (Comb H to S) and Figure 24 (Comb S to H) exhibit a distinct, measureable difference between the two RTDs.

To determine whether the interdigitated configuration response is to be expected, FEA simulations were performed on the three nanofilm configurations. Figure 25 presents the average temperature differences between the sample RTD (orange hash bar) and sample RTD (green solid bar) measured experimentally. This representation of the data clearly shows that the comb S to H configuration generated a slightly larger temperature difference than the comb H to S configuration and that the interdigitated

device produced the smallest temperature difference of the three configurations.

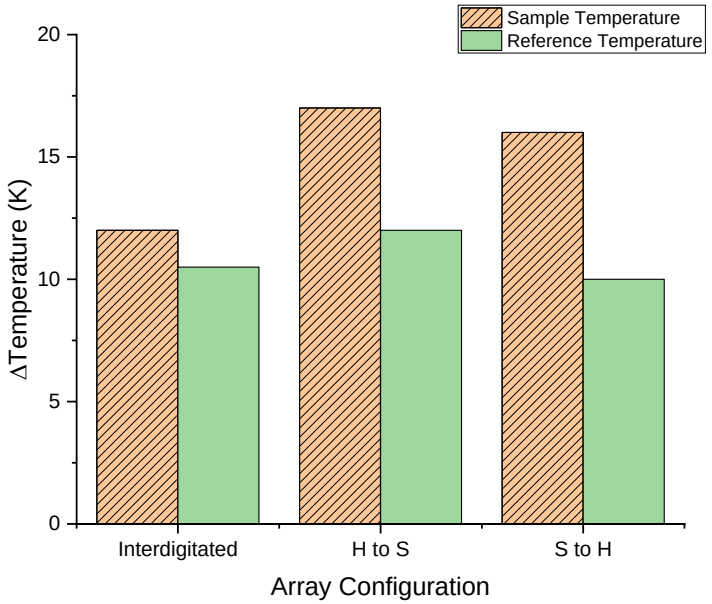


Figure 25. Experimental Temperature Response of 3 Nanofilm Configurations.

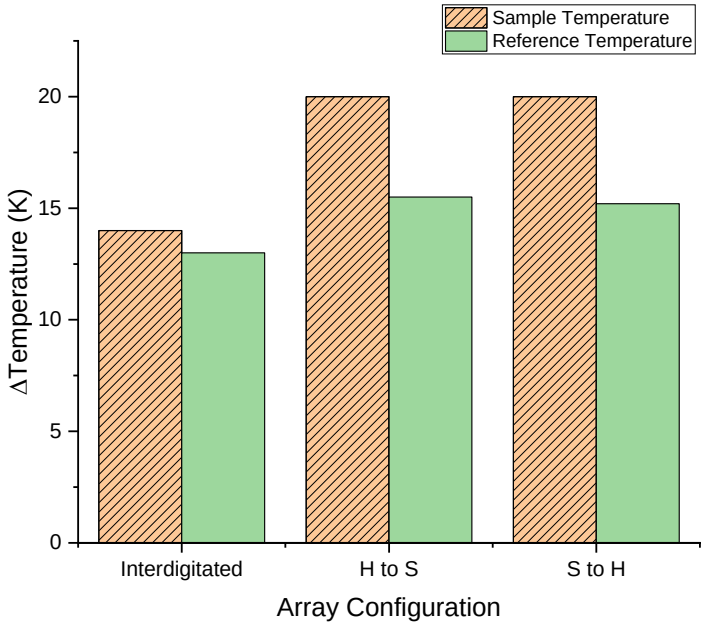


Figure 26. FEA Simulated Temperature Response of 3 Nanofilm Configurations.

The results of the FEA simulations on the three device configurations is shown in Figure 26, which predicted that the interdigitated device would produce the smallest temperature difference between the sample RTD and reference RTD as compared to the two comb devices. Accordingly, the comb S to H configuration was selected for the fabrication of all the test devices in this study. Further, the advantage of the comb S to H configuration over the comb H to S is the ability to determine the resistance value of each array configuration by subtracting the reference RTD resistance from the sample RTD resistance. In other words, it is possible separate out the heat conduction due to the nanowire array from parasitic heat losses experienced by both RTDs. Lastly, the comb S to H configuration allows additional flexibility in e-beam writing to achieve different pitches in the array that are more difficult to achieve with the interdigitated design.

4.6 Cobalt Nanowire Array Using FEBID

An additional approach for nanostructure generation was investigated in this study. The heater and two RTD sensor were patterned and metallized in the same manner as previously described, but the nanostructure array was generated using focused electron beam-induced deposition (FEBID). In this process, the SEM's electron beam directly "writes" the nanostructure array using the gas-injection system (GIS) of the SEM, as shown in Figure 27. On the SEM used in this study, several organo-metallic precursor materials are available for deposition, including platinum, tungsten, and cobalt. Cobalt was selected for this study due to its shorter mean free path (11.8 nm) and is believed to reduce the resistivity size effects experienced in other traditionally-used interconnect materials such as copper.[27, 101]

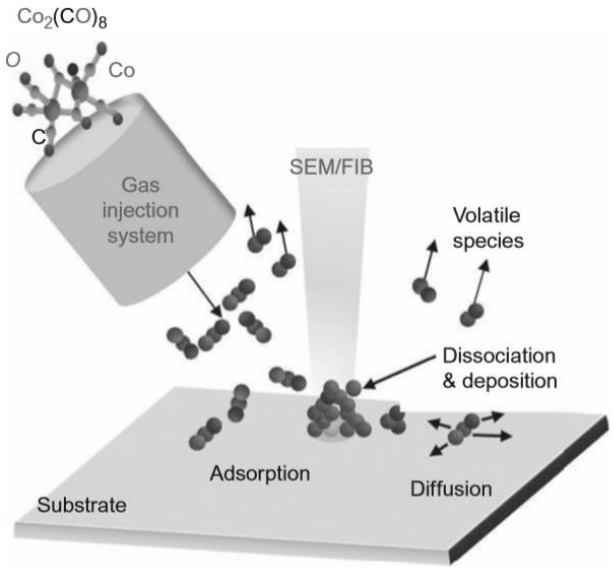


Figure 27. Schematic of Focused Electron Beam Induced Deposition (FEBID)[11]

Details of the cobalt study are presented in the Appendix. Investigation of cobalt nanowires via FEBID was curtailed due to the inability to eliminate the cobalt overspray and potential damage to the sensitive SEM stage components during cobalt usage.

4.7 Electrical Testing

The test devices were electrically interrogated using a Cascade Summit 12000 Probe Station (Cascade Microtech, Beaverton, OR) coupled with a Keysight Technologies B1500A Semiconductor Device Analyzer (Santa Rosa, CA). This arrangement allowed for simultaneous probing of the heater and two RTD sensors using two high-power source/monitor units (SMU) and two high-resolution SMUs. An Advanced Temperature Test (ATT) Systems Chuck controller provided constant temperature control to the wafer coupon during testing. Table 4 details the probe and SMU assignments used in the testing.

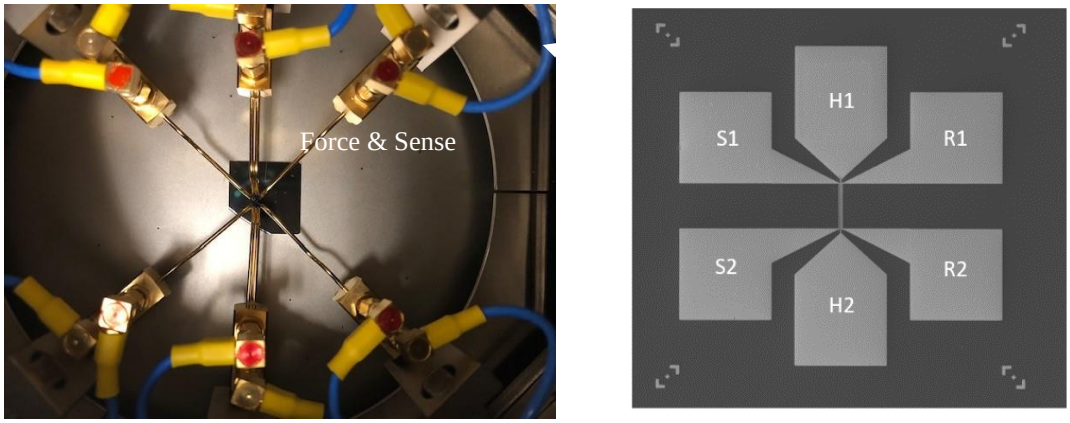


Figure 28. Electrical Interrogation of DUT and Configuration.

Figure 28 presents the configuration of the probes and SMUs during testing, with actual probe placement on the device shown in the schematic of Figure 28. As evidenced by the photo, simultaneous probe testing of the device is quite challenging due to the very tight confines of the device geometry and the dimensions of the probes and positioning units. Care was taken to ensure that each probe and associated wiring did not contact or impede an adjacent probe.

Table 4. SMU Configurations for Electrical Testing

Probe	**Probe Type**	**SMU**	**Mode**
Heater (H1)	Kelvin	HR3 (force & sense)	Var I
Heater (H2)	Kelvin	HR4 (force & sense)	Common
Sample RTD (S1)	Single	HP1 (force)	Var I
Sample RTD (S2)	Single	GRND	Ground
Reference RTD (R1)	Single	HP2 (force)	Var I
Reference RTD (R2)	Single	GRND	Ground

4.8 Kelvin Probes vs. Single Probes

Kelvin probes were used to source the drive current to the heater to ensure an accurate, consistent heater response with each device tested. Derived from the accepted four-point probe approach, Kelvin probes employ one line to supply the current to the device (force) and a separate line to measure the voltage drop across the device (sense). Since the sensing line is not conducting current, there is no V=IR related voltage drop due to the inherent cable resistance. Figure 28 shows the force and sense lines in close proximity contacting the heater, as highlighted in the photo. Testing was conducted to compare the measurements taken with the Kelvin probes with the single probes in order to measure the cable resistance, as shown in Figure 29. From the slope of

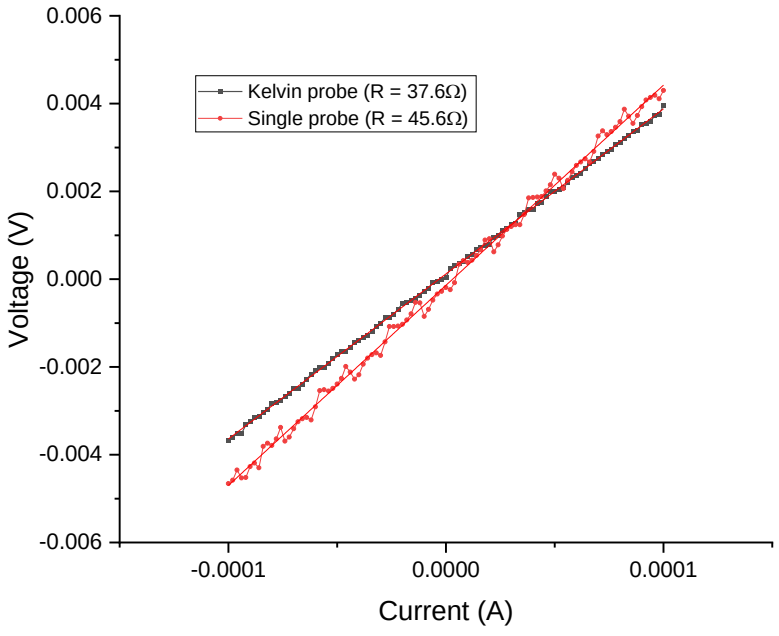


Figure 29. Comparison Between Kelvin and Single Probe.

the I-V sweeps, the resistance from the Kelvin probe was 37.6 Ω, as compared to the single probe value of 45.6 Ω, a difference of 8 Ω. This difference may be attributed to residual resistance from cabling and probe contact resistance. It is also important to note the increased scatter of the single probe measurement as compared to the Kelvin measurement. In order to provide a consistent heater response for a given current sweep, while also measuring the associated voltage for determining resistance (and hence temperature), it was decided that the Kelvin probes would be used for driving current through the heater for each test. This is intended to allow for more accurate comparisons to be made between and among different test device geometries.

Since a full set of three Kelvin probe pair assemblies was not available, both the sample RTD and reference RTD were driven by single tungsten probes with a very low current (1mA) going to a common ground. This low current was selected to avoid self-heating and to facilitate measurement of the voltage drop across each RTD by reducing noise in the signal.

4.9 I-V Sweep of the Device Heater

The wafer coupon was loaded onto a vacuum chuck and the testing temperature was set to room temperature (26.8°- 30°C) and 100°C. This elevated testing condition was selected to approximate operating temperatures in-service in a microelectronic (logic) device. All testing was conducted at atmosphere. Prior to temperature testing, the chuck temperature was allowed to reach equilibrium for at least 10 minutes prior to the commencement of testing. Once loaded, each probe tip was landed on the DUT (device under test), with care taken to achieve good contact, but not “dig” into the substrate.

The probe station has an option to circulate clean dry air (CDA) over the chuck

during elevated temperature testing to improve the uniformity of the temperature across the platen. However, early testing suggested that the air flow of the CDA impacted the measured temperatures in the test structure by increasing the variability of the measured voltages. Accordingly, the circulated air was shut off during testing.

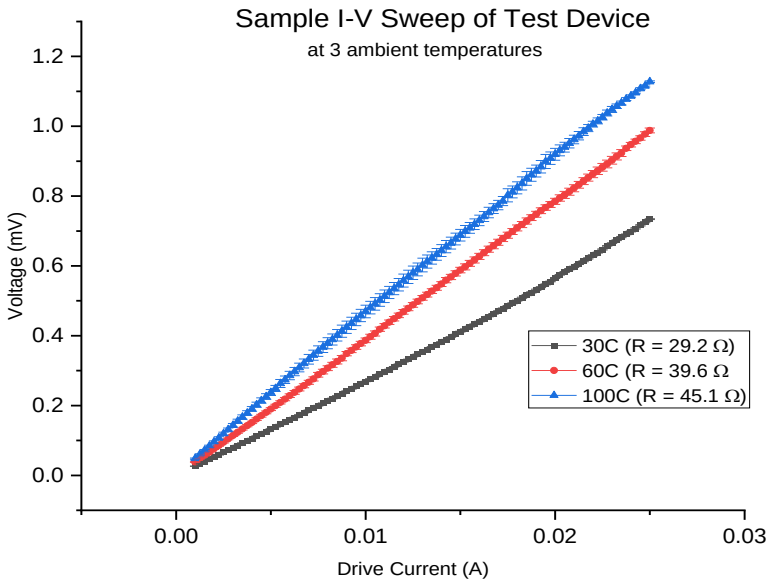


Figure 30. Sample I-V Sweep of Test Device

The Keysight Semiconductor Device Analyzer was used to control the device testing. A specific I-V sweep was programmed for the heater depending on the deposition thickness of the device tested. Several different test and sampling protocols were evaluated to examine ramp rates and delay/ hold times between current steps. The voltage change across each RTD was recorded throughout the entire I-V sweep of the heater.

Once the probes were in position, the I-V sweep was initiated through the heater after a 2 s delay. The current was increased in 250 µA steps, which means that the current incrementally increased every 0.11 s, corresponding to a hold time for each measurement.

This is important information in order to characterize the time domain of the testing, as noted in Chapter 3. The heat diffusion time in the test device can be estimated by $L = \sqrt{Dt}$, where D= 8.7 x 10^{-7} m^2/s is the thermal diffusivity of the substrate (SiO_2), and L is the distance between the heater and sensors (approximately 1 µm) or the heater and substrate (2 µm). This yields an estimated heat diffusion time of 1 - 5 µs, which is a significantly shorter period of time than the incremental current increase. Based on these values, we can assume that the testing is a "quasi-steady-state" condition, since it can be assumed that the temperature equilibrates before each subsequent current increase. In effect, each I-V sweep represents 98 individual quasi-steady-state measurements, spanning 0 mA to 25 mA (for 100 nm thick devices) and 0 mA to 15 mA (for 50 nm thick devices).

A series of sample I-V sweep is shown in Figure 30, where a drive current is imposed upon the heater of the device at three ambient testing temperatures. The difference in voltage response among the three testing temperatures is apparent, where

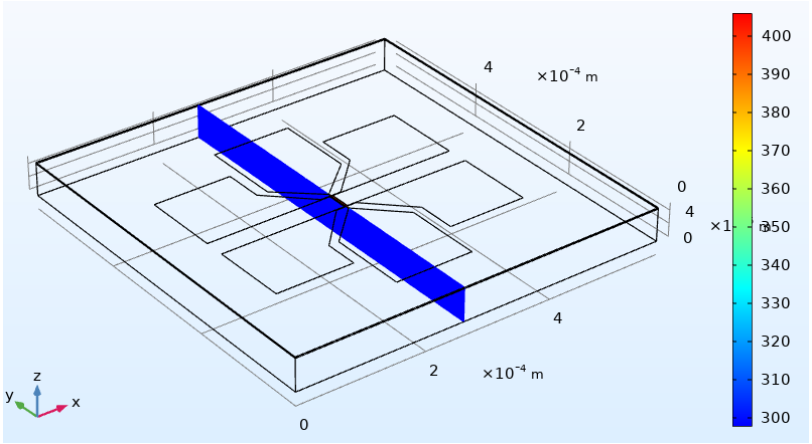


Figure 31. Cut-plane Temperature Simulation Along Heater Trace.

resistance, the slope of the I-V curves, increases as ambient temperature is increased.

This response expected since the increased temperature results in a higher resistance in the gold due to increased mobility and scattering of carriers. Also, increasing the testing temperature results in increased measurement variability as shown in the error bars of the Figure 30.

Elevated temperature testing on electrical probe stations is fraught with opportunities to introduce variability. As the platen is heated, both the platen and wafer coupon experience thermal expansion which impacts the contact pressure of the probes contacting the test devices. Despite careful manipulation of probes, it is difficult to achieve consistent contact of the probes.

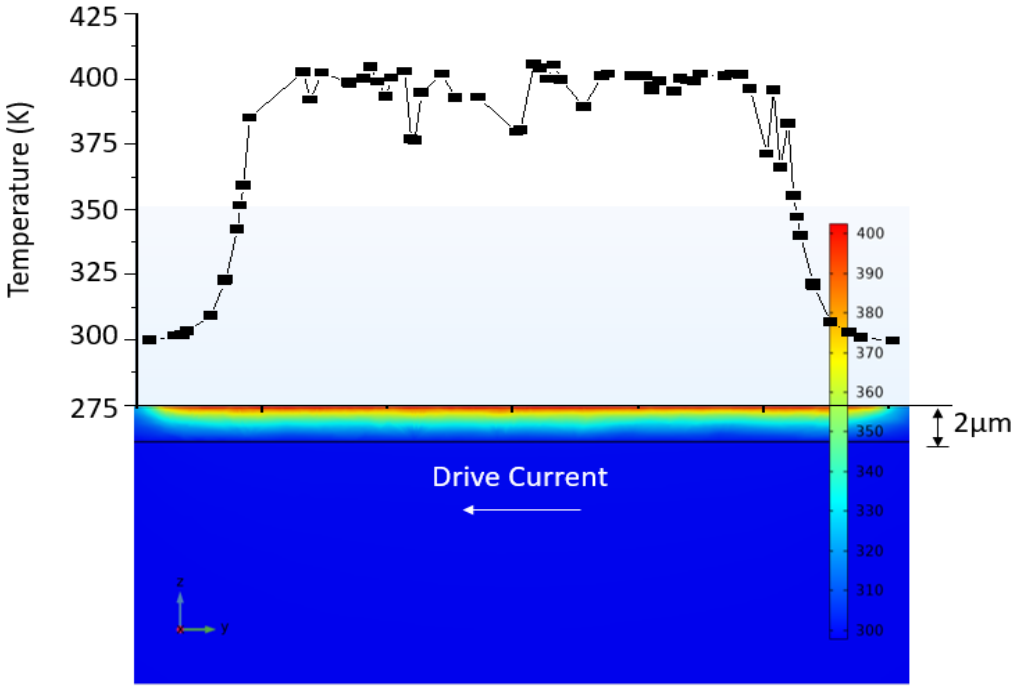


Figure 32. Cut-plane Through the Heater.
Average Surface Temperature Response (above)

The temperature along the length of the heater trace varies for a given drive current. Figure 31 presents the FEA geometry for a simulation of the temperature

distribution along the length of the heater trace for a drive current of 25 mA on a device with 100 nm thickness of Ti/Au. In the simulation, a cut-plane was introduced along the heater trace. The temperature distribution into the substrate and along its length is illustrated in Figure 32. The color-coded image represents the temperature into the substrate, with the 2 µm oxide layer denoted. The graph along the top of the image is the average surface temperature of the heater trace along its length, extending between the two contact pads, with positions shown by vertical dashed lines. The contact pad to the right of the image is the terminal, with the contact to the left serving as ground. The graph shows that the temperature is close to ambient where the heater meets the two contact pads, and quickly increases in the middle of the trace to a maximum temperature of 403K, where it holds steady along the full length of the heater trace.

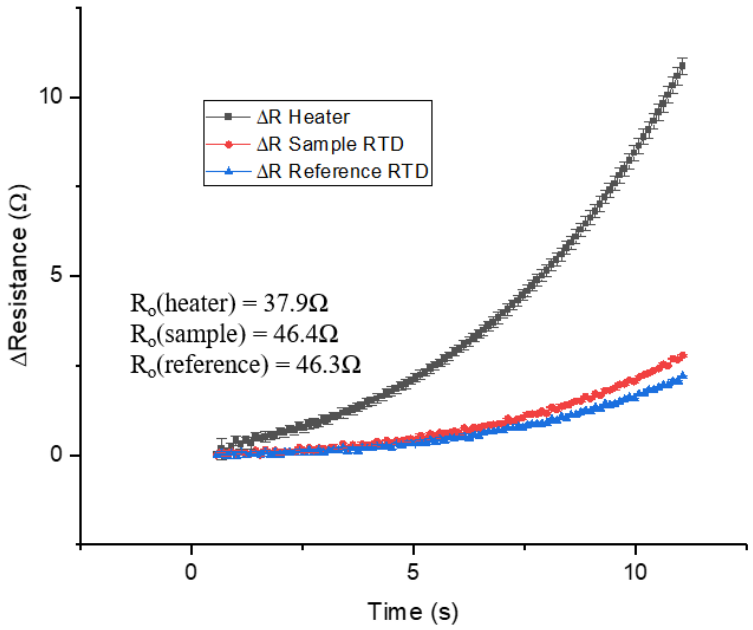


Figure 33. Change in Resistance vs. Time, Fine NW Array at Room Temperature.

Some temperature variability is observed in the central portion, possibly due to the

presence of the nanowire array extending from the sample RTD towards the heater. The observed variability may also be related to the intersection of the cut plane with mesh elements.

Under a given heater drive current, the voltage change across each RTD is measured. This voltage change, divided by the low 1 mA current applied to each RTD, yields a resistance value at each step of the I-V Sweep. The change in resistance experienced by the heater and each RTD at room temperature is shown in Figure 33 for 100 nm thick Ti/Au sample with a fine pitch nanowire array of 160 nm wide wires. The nanowire array is a comb S to H configuration, as discussed in Section 4.5.

The steep change in the resistance of the heater trace (black) is indicative of heating due to the applied current. The sample (red) and reference (blue) RTD response also increases throughout the sweep, as heat is transferred through the substrate via conduction to the two RTDs and is measured as a resistance change. The sample RTD is shown to have a slightly greater change in resistance than the reference RTD. The nanowire array serves as a conduction path to promote heat transfer to the sample RTD as compared to the reference RTD. The sample and reference RTD begin to reach a measurable difference in resistance values at 18 mA, or approximately 7.5 s into the I-V sweep. The difference in resistance between the two RTDs continues to increase until the peak sweep drive current of 25 mA is reached. The determination of this peak value is discussed in the next section. For each series of nanowires and nanofilms studied, between 3 and 5 sweeps were performed to establish measurement error. Occasionally, a device would require multiple sweeps after the probes landed on the device to ensure the probes were properly “seated” on the contact pads.

Identical sweeps were conducted on this sample with a testing temperature of 100°C and resulted in a similar response trend of the heater and two RTDs, except the resistance changes experienced by all three components was higher than the room temperature conditions.

Table 5. Change in Resistance at Room Temperature and 100°C

	ΔResistance @ 25 mA (Ω)		
Temperature (°C)	Heater	Sample RTD	Reference RTD
30	10.9	2.8	2.2
100	13.1	3.2	2.6

The comparison of the data is shown in Table 5, with the change in the resistance of the 100°C testing condition consistently higher than the room temperature testing condition for the same current sweep. The elevated resistance with increasing temperature is due to increased energy of the heat carriers, resulting in increased collisions. These collisions, in turn, release more energy in the form of heat, so the resistance is further increased.

4.10 Failure Current Density Determination

The selection of the I-V parameters also included the determination of the maximum drive current possible to achieve sufficient heating, not to exceed the failure limit of the device or microstructural changes in the material.

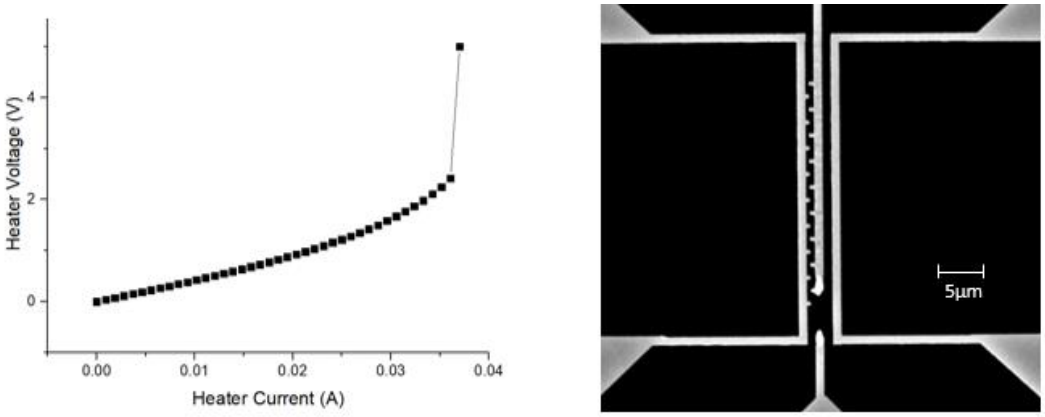


Figure 34. Heater Failure due High Current Density.

Figure 34 illustrates the effect of exceeding the allowable current density prior to material failure. The graph to the left illustrates how the curve becomes non-linear with increasing drive current until the current density reaches failure at 3.7 x 10^{11} A/m^2, consistent with the findings of other researchers evaluating gold nanowires. [102-105] The failure shown in the photo to the right shows a characteristic failure due to electromigration, common failure mechanism in electronic materials.[106]

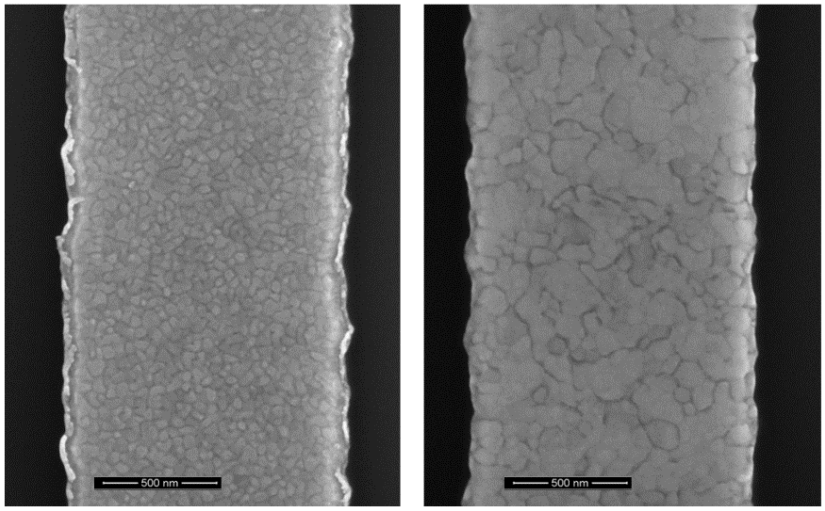


Figure 35. Microstructural Comparison.
Reference trace (left) and Heater trace (right) after failure

Electromigration can be described as “the movement of thermally-assisted ions under an electric field.”[104] When the heater is electrically-stressed, the metal heats up and the atoms become more mobile. The atoms move in the direction opposite of the current flow. As the ions move along the length of the trace, voids are formed which coalesce into tiny cracks, leading to eventual failure.

Figure 35 provides a comparison between the microstructure of the reference RTD trace (left) and the heater trace (right) after failure. The microstructure of the RTD is a uniform, equiaxed grain structure, while the heater microstructure shows large, uneven grains with small fissures along the grain boundaries. The change in the microstructure of the heater trace under an applied current can help reveal the temperature achieved in the trace. Significant microstructural changes can be observed in evaporated gold films when temperatures are in excess of 300°C. [107] In the case of devices used in this study, electromigration causes a non-uniform temperature distribution across throughout the heater trace, confounding the ability to accurately measure the thermal response of the RTDs for a given drive current. Moreover, electromigration eventually leads to device failure. In the case shown in Figure 34, the initial heater resistance at room temperature was measured to be 31.4 Ω. The resistance steadily rose as drive current increased, reaching 60.5 Ω resulting in a temperature of 721K at 34 mA drive current. The heater resistance then spiked to 142.9 Ω at 35 mA, with a temperature of 1914K before failure, consistent with the 1948K melting point of gold.

4.11 Determination of the Temperature Coefficient of Resistance

As noted previously, the data generated from the electrical testing is recorded by the Keysight Semiconductor Device Analyzer. The collected data includes the drive current applied to the heater as well as the potential drop across heater and the two RTD sensors. From this data set, the resistance values of the heater and the two RTDs can be calculated and used to determine the temperature increase due to Joule heating. Critical to this calculation is the determination of the linear temperature coefficient of resistance.

With the exception of very low temperatures, the resistivity of metals varies linearly with temperature. Accordingly, the resistivity function ρ(T) can be approximated using a Taylor expansion at a given temperature T, according to

$$\rho(T) = \rho_0 + \alpha(T - T_0) + (\frac{1}{2})\beta(T - T_0)^2 \tag{14}$$

where T_0 is a reference temperature, such as ambient in these experiments, α and β are expansion coefficients. When T is close to T_0, the first degree Taylor polynomial is sufficient for describing the temperature dependence.

$$\rho(T) = \rho_{T_o} + \alpha\rho_{T_o}(T - T_o) \tag{15}$$

Assuming the resistor geometry does not change over the temperature range of interest, resistivity is readily converted to the measured quantity resistance. Measure the reference temperature T_0, R_0 , and R allows estimation of the resistor temperature.

$$T = To + \frac{R - Ro}{\alpha Ro} \tag{16}$$

Calibration of a given heater is carried out to determine α. A series of reference

measurements is conducted on the heater of the test device with the sample affixed to the

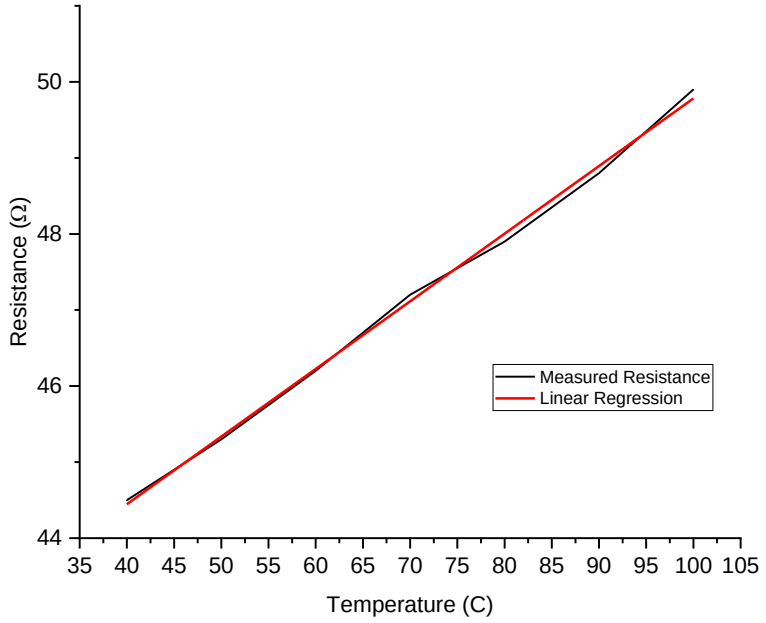


Figure 36. Resistance vs. Temperature for TCR Determination.
100 nm thick Ti/Au

heated platen held at a temperature varied across the range of interest. Resistance is measured using Kelvin probes to minimize the impact of contact resistance. To determine resistance, an I-V sweep is conducted from -5 mA to 5 mA at 100 µA steps. The currents are sufficiently low to minimize Joule heating in the heater structure. The TCR value can be calculated by dividing slope of the linear fit shown in Figure 36 by the initial resistance value at room temperature. The TCR value for bulk gold is 3.7×10^{-3}/K [108], while the TCR value in the current study is 2.2×10^{-3}/K. This calculated value for TCR of nanoscale gold is consistent with the findings of other researchers [102, 106, 109]. In metals, it is expected that the resistance, and resistivity, would increase with increasing temperature due to increased electron-atom and electron-electron collisions. [110] The significant reduction of TCR values in nanoscale studies as compared to bulk is likely

related to surface scattering effects due to the increased surface to volume ratio with diminishing dimensions.[111]

A similar temperature series was conducted for the 50 nm thickness Ti/Au test devices, and a TCR value of 2.1 x 10^{-3}/K was calculated.

4.12 Summary of Chapter

In this chapter, the fabrication of the test devices and the electrical testing methodology was presented. Much of the work was accompanied by FEA simulations to guide design decisions. Specific testing protocols and limitation were established. This chapter lays the foundation for performing the research and analyzing the results.

5. MATERIAL CHARACTERIZATION AND SIMULATION STUDIES

Figure 37 represents the experimental space for test conditions in this study. Three main variables were considered: nanostructure width, deposition thickness, and testing temperature. Testing temperature and deposition thickness were discreet values, while nanostructure width was a range of values from 74 nm to 720 nm (nanofilms).

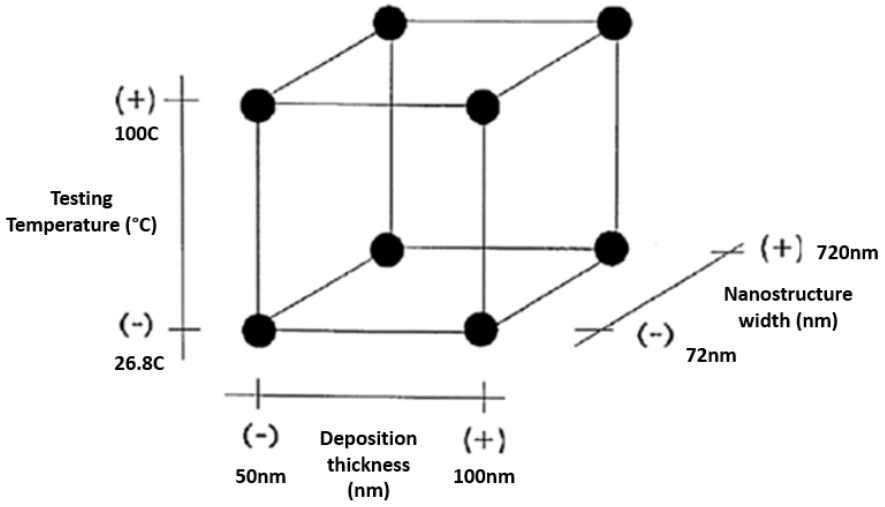


Figure 37. Representation of Testing Conditions.

Several test devices were fabricated on each wafer coupon. For a given nanostructure geometry, numerous test devices were fabricated to determine testing error. Additional factors were also evaluated, including the density of wires in the array, which will be discussed in Section 5.3 and 6.2, and the configuration of the arrays which was discussed previously in Section 4.5.

5.1 SEM Imaging

Test devices were imaged in the SEM to measure the width, length, and spacing dimensions of each trace and nanostructure array. Additionally, the deposition thickness of each wafer coupon was measured using two methods: stage tilt and focused-ion beam (FIB) cross-section. The stage-tilt method is shown in Figure 38. These critical measurement values were later inputted into the FEA software geometry for simulation studies for each unique test device.

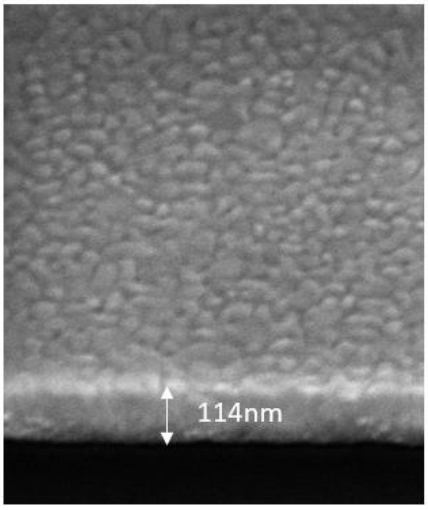


Figure 38. Evaporated Ti/Au Film Thickness Measurement.
45° tilt on contact pad

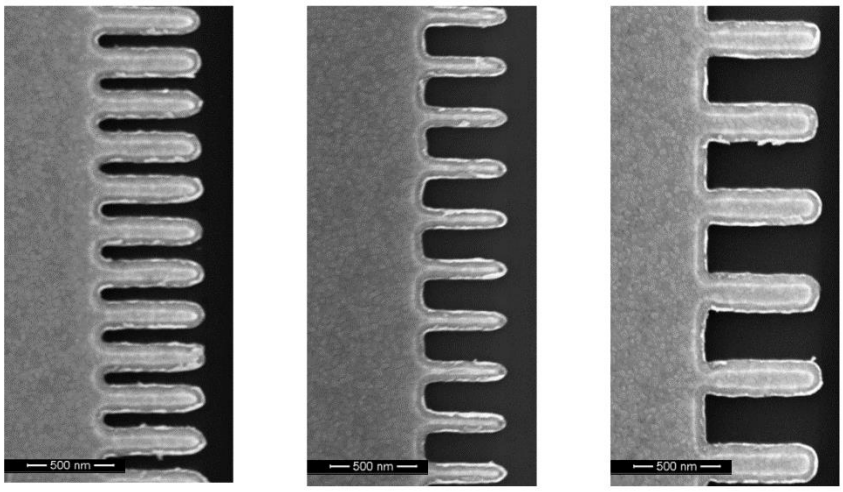


Figure 39. Three Pitch Configurations of Nanowire Arrays.

Within this experimental space, different pitch values were fabricated for the smaller width (<175nm) nanowire arrays. Pitch refers to the center-to-center distance between nanowires in the array. Figure 39 compares three different pitch configurations for the nanowire arrays.

In the narrow pitch configuration shown on the left, the total array consists of 128 individual nanowires, while the wider pitch array configurations consists of 68 and 62 individual nanowires, respectively.

Besides nanowire arrays, nanofilms were also fabricated in this study. Figure 40 presents an example of a nanofilm with a width of 683nm. Nanofilm widths in this study range from 640nm to 720nm, with 32 nanofilms per array. The addition of nanofilms in this study was to demonstrate the efficacy of this direct testing method of thermal conductivity on thin film materials while spanning a wide range of widths from micro- to nano-scale.

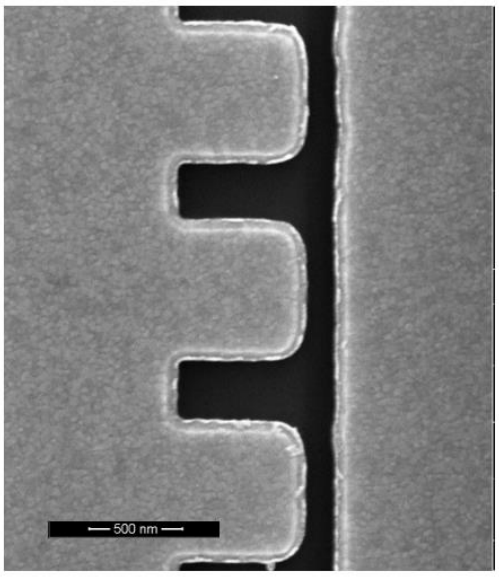


Figure 40. Nanofilm Array.

5.2 Grain Size Analysis

In addition to dimensional analysis of each test device, grain size analysis was also performed. TIFF (Tagged Image File Format) SEM images of the two deposition thicknesses, 100 nm and 50 nm, were imported into a data visualization and analysis software program called Gwyddion. Using various filtering and measuring tools, the mean grain size of the 100 nm Ti/Au deposition was determined to be 35 nm ± 4 nm, while the 50 nm Ti/Au deposition was 27 nm ± 5 nm. As evident in Figure 41, the

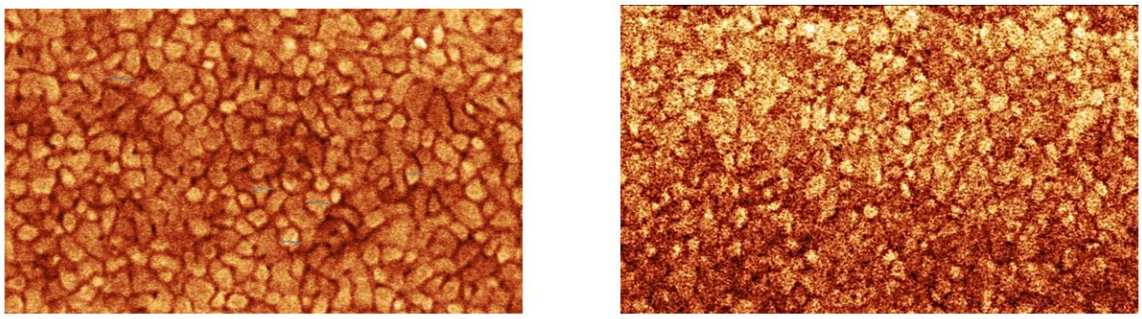


Figure 41. Grain Size Analysis.
100 nm Ti/Au deposition (left) grain size = 35 nm,
50 nm Ti/Au deposition (right) grain size = 27 nm

100 nm deposition microstructure consists of relatively uniform, nodular grains, while the 50 nm deposition, has a finer overall grain size with increased variability in size. As noted previously in Chapter 2, grain size and deposition thickness are correlated, where grain size is shown to increase with increasing deposition thickness. The finer grain size of the 50 nm deposition translates to increased grain boundary area, which serve as increased scattering sites for thermal carriers as compared to the coarser-grained 100 nm deposition conditions. Given that measured grain sizes are comparable to the MFP of gold is 38.9 nm[26], this is an important parameter and will be discussed in the interpretation of the results in Chapter 6.

5.3 Effect of Nanostructure Dimension on Thermal Response

Several different nanostructure dimensions were considered in this study. The change in dimension of the individual nanostructures impacts the "fill factor," or the amount of Ti/Au material residing in the gap between the sample RTD and heater of the tests device. The length of the individual nanowires also impacts that fill factor. Intuitively, higher fill factor will increase the temperature rise in the sample-side sensor because the conductance is in proportion to the net cross-section area.

The following set of data was generated on a single wafer coupon with multiple test devices, as described in Section 4.3 and shown in Figure 18. This permits each device to be fabricated at the same time for achieving identical processing conditions. During the metallization process, a 114 nm ±5 nm thick layer was deposited for the devices shown in Figure 38. The Ti thickness is estimated to 5 nm, while the Au thickness approximately

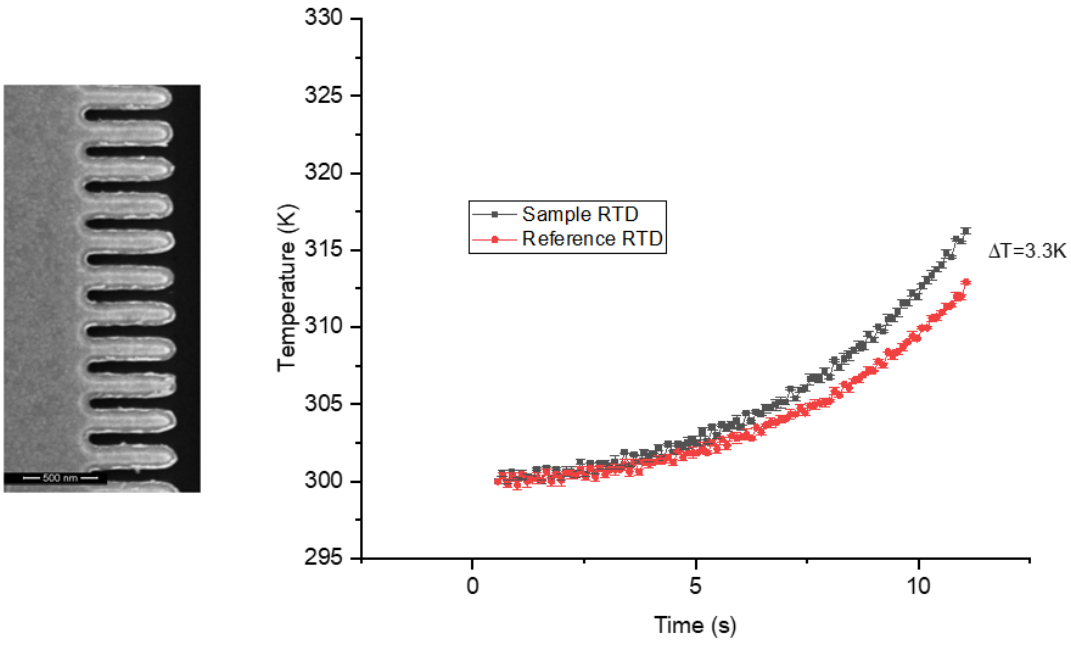


Figure 42. Thermal Response of 161 nm Nanowire Array Fine Pitch.
at Ambient = 298K

109nm. The devices had different nanostructure arrays geometries, from 161 nm width wires to 694 nm width nanofilms.

The temperature response of the two RTDs with a fine pitch, 161 nm width nanowire array is shown in Figure 42. The temperature values were derived from the measured resistance values from multiple I-V sweeps and the relationship expressed in Equation 16, with an experimentally derived TCR value of 2.2 x 10^{-3}/K. The sample RTD experiences a temperature increase of approximately18K over the 11 s duration of the sweep, while the reference RTD has a temperature increase of 14.5K, with a nominal temperature difference of 3.3K between the two sensors.

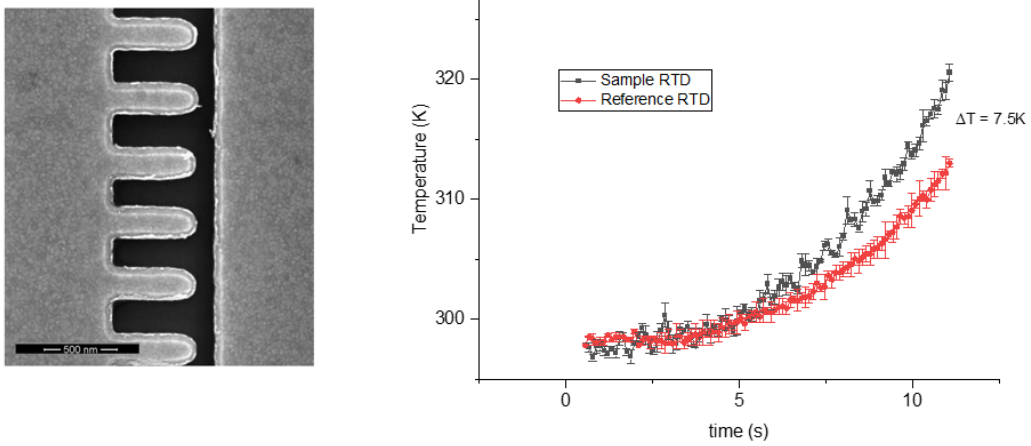


Figure 43. Thermal Response of 230 nm Wide Nanowire Array.
at Ambient = 298K

The thermal response of 230 nm wide nanowires is shown in Figure 43 with a temperature rise of 21K and 14K for the sample RTD and reference RTD sensors, respectively, and maximum temperature difference between the two sensors of 7.5K. The larger temperature difference observed in the 230 nm wire array as compared to the

161nm wire array which suggests that heat transfer is dependent on the width of the nanowires in the array, regardless of the higher fill-factor shown in Figure 42. The effect of fill factor will be further discussed in Section 6.2.

The response of the 694 nm nanofilm array as shown in Figure 44. A temperature difference of 8.9K was achieved between the sample and reference RTDs, suggesting an even greater thermal conductance than the 230 nm wide wire array.

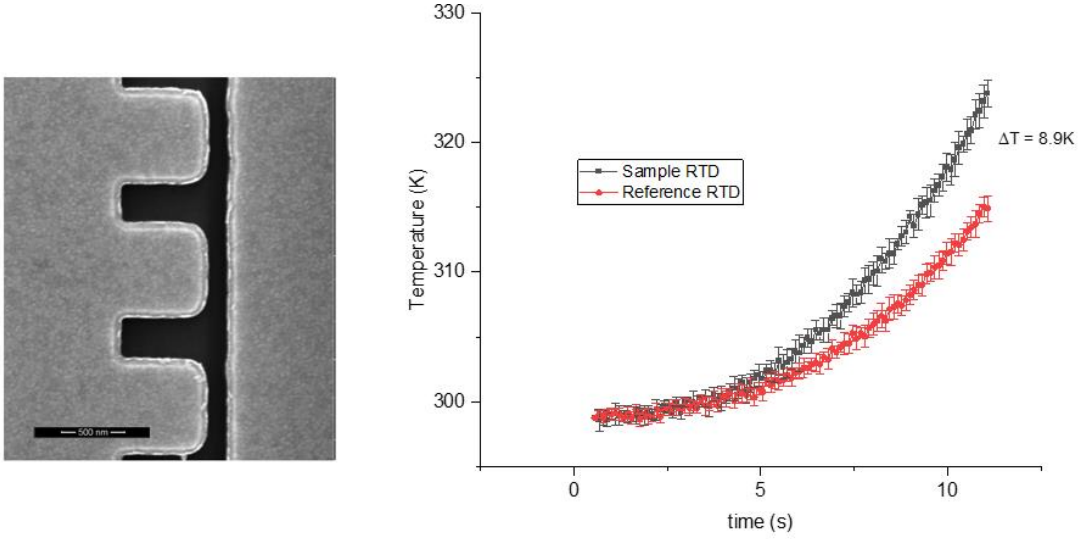


Figure 44. Thermal Response of 720 nm Nanofilm Array.
at Ambient = 298K

Similar responses were observed at the elevated testing temperature of 100°C. Multiple test structures were evaluated in a similar fashion, with nanowire widths ranging from 74 nm to 720 nm (nanofilm), with varying pitches for nanowires less than 170 nm. The effect of elevated testing temperature is explored in Section 6.3.

5.4 COMSOL® Simulations of Test Devices

The experimental data generated from the electrical testing was used to estimate the thermal conductivity of the different nanostructure array geometries using COMSOL® Multiphysics (version 5.4), a finite element analysis (FEA) software. FEA is

a numerical method to calculate displacements or thermal changes under known applied load(s) or heat flux(es).[112] A computer-aided design (CAD) file or component geometry is imported into the FEA code which "discretizes" the components into a mesh of finite elements. In COMSOL®, there are several different options for automated mesh generation depending on the physics and the desired solution accuracy. The nodes of the mesh are positioned in key locations throughout the geometry, including at material interfaces, at boundary points, and at locations where loads or fluxes are applied. Within each element, the node values are estimated using approximate numerical solutions based on the partial differential equations (PDE) of the physics involved in the study.[113] Equilibrium principles are applied to each element until an overall global equilibrium equation is established. Constraints, boundary conditions, and material properties are applied to the global equilibrium equation which reduces the numbers of degrees of freedom of the problem. The output from the global equilibrium equation is then post-processed to test the validity of the model to experimental results.

In this research, a parameter estimation study in COMSOL® was performed. This type of study allows the estimation of the value of a parameter based on inputted experimental data. This is essentially an inverse modeling problem, whereby a value of a parameter or set of parameters is determined which results in the best match between the simulated results and the experimental data. This is achieved by minimizing the sum of the squares of the differences between the simulated and experimental data sets. COMSOL® provides several different optimization algorithms to solve a least-squares problem with time-dependent measurements.[114]

The precise dimensions of the test devices, as described earlier in this chapter,

were used to generate a unique geometry for each simulation. A 3-D geometry was created as shown in Figure 45, with the Ti/Au test device atop a 2 µm layer of

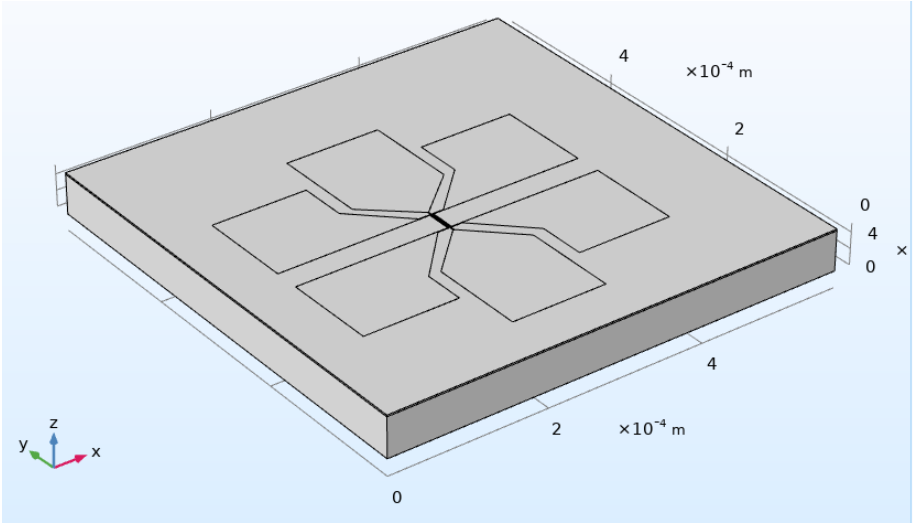


Figure 45. COMSOL® 3-D Geometry of the Test Device

silicon dioxide layer and a silicon wafer coupon. Once the space dimension was established, the physics modules were added to the model. The drive current applied to the device results in Joule heating, so both the Heat Transfer and AC/DC modules were enabled in the model to address the two-way coupling of resistance heating. Next, the type of study was designated as "time-dependent" to reflect the current sweep imposed on the heater, with the start time, stop time, and time intervals defined.

5.5 Meshing of the Geometry

There is a considerable range of component dimensions within the test device, from the 120 µm square contact pads to the 5 nm thickness of the titanium adhesion layer. This poses difficulties for FEA simulations due to the number of calculations performed at each mesh node and boundary. Accordingly, the discretization of the mesh

must be selected to accommodate the different dimension scales, while achieving appropriate result accuracy. For example, if a coarse mesh is selected that has mesh elements larger than the dimensions of components of the device, the contribution of these small dimension components to the problem solution may not be realized. Similarly, if a very fine mesh is selected with elements significantly smaller than a component, needlessly excessive runtime will be required to converge a result. To address this concern, two different approaches were considered to model heat transport in the device.

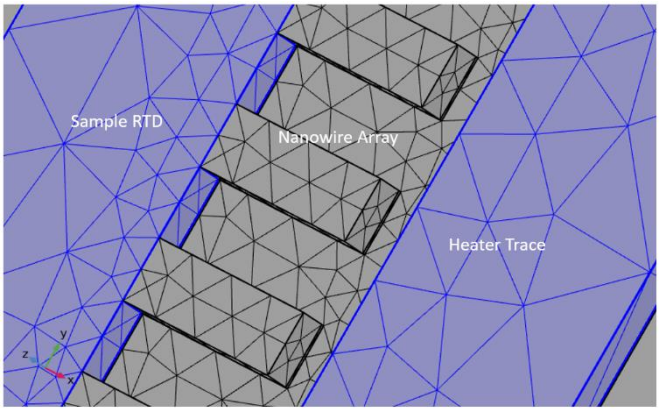


Figure 46. Meshing of the Test Device with Two Distinct Layers

For the first approach, the test device was constructed as two discrete layers: the 5nm Ti layer and the thicker (50-100 nm) Au layer. The meshing of this configuration is shown in Figure 46, with a portion of the nanowire array positioned between the sample

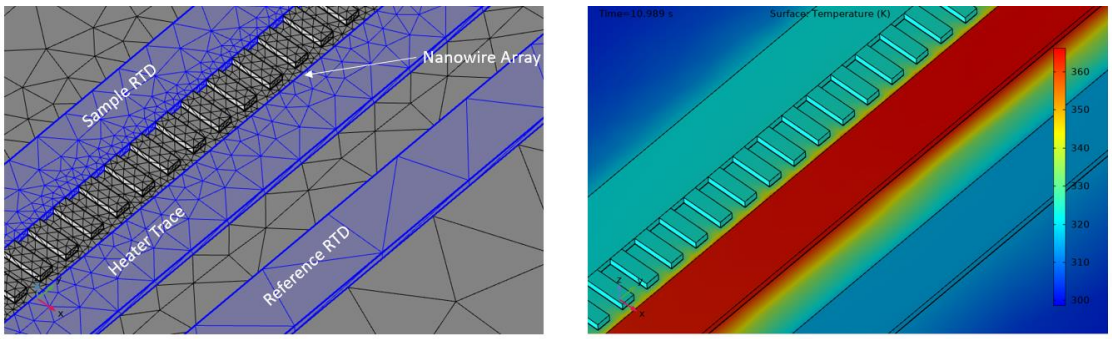


Figure 47. Two Distinct Layer Mesh Configuration and Temperature Distribution

RTD and heater trace (in purple). The image is tilted so that the titanium adhesion layer is visible at the bottom of each nanowire. Very small elements were generated in the vicinity of the nanowires, particularly in the 5 nm titanium layer array with a high density of very small elements.

A larger overview of the meshing configuration shown in Figure 46 and the resultant temperature distribution after the simulation is completed is shown in Figure 47. The orientation and meshing of the two RTD sensors, nanowire array, and the heater are shown in the image to the left. This view provides a good comparison of the meshing differences of the device components, with a higher density of small elements in the area of the nanowires and larger elements in the sensors and oxide substrate. The image to the right in the figure is the temperature distribution of the device components under an applied drive current to the heater. The analysis of the simulation results will be further discussed in the next section. In general, this stacked “sandwich” method proved cumbersome and the solution would often not converge due to the disparity of meshing sizes for the various layers and features of the geometric domains.

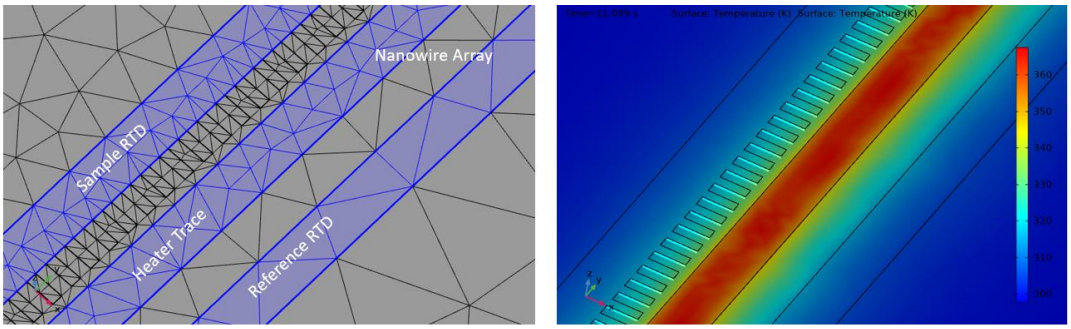


Figure 48. Thin Structure Model Mesh Configuration and Temperature Distribution

A second approach to construct the device involves modeling the test device as a thin structure, as shown in Figure 48. The thin structure approach in COMSOL® is designed for models with large aspect ratios, such as the test device, where the substrate dimension is significantly larger than the test device itself. In this method, the model considers the thin layer as a boundary, as opposed to a series of discrete layers.[115] By using this approach, the mesh generator is capable of addressing geometries with vastly different thicknesses, as is the case with the current study. Essentially, the thin structure approach converts a 3-D heat transfer problem into a 2-D boundary problem with thickness. This is expressed in the 3-D heat equation:

$$\rho C_p \left(\frac{\partial T}{\partial t}\right) + \rho C_p u \cdot \nabla T + \nabla \cdot q = Q \tag{15}$$

where u is the velocity field, q is the heat flux by conduction, and Q is heat source [W/m^3].

For the 2-D boundary with thickness, this relationship becomes the following:

$$d_s \rho C_p \left(\frac{\partial T}{dt}\right) + d_s \rho C_p u + \nabla_s \mathrm{T} + \nabla_s \cdot q_s d_s = Q d_s \tag{16}$$

Where d_s is the thin layer thickness. The gradient and divergence function, $\nabla_s \mathrm{T}$ and ∇_s, are either tangential or normal, depending on the type of thin structure considered. The

subscript “s” is a “reminder that the variable lives in the product space of the thin structure.” [113]

A comparison between Figure 47 and Figure 48 highlights some key differences between the two approaches. First, the thin structure meshing of Figure 48 is less complex and yields results that easily converge in a relatively short period of time. When considering the temperature distributions images, the model with the two distinct layers shows a marked difference in temperature between the sample RTD and the reference RTD, while the thin structure model does not exhibit as large a disparity. The average temperature of the sample RTD in the two simulations was comparable, but the average temperature of the reference RTDs was quite different. When the two simulations were compared to the experiment results, the thin structure temperature distributions of the sample and reference RTDs were in better agreement with the experimental data. This suggests that the thin structure model provides better agreement with the overall thermal state of the device during testing.

Within the thin structure option of COMSOL®, there are several ways to characterize the structure, including a thermally thin approximation, and thermally thick approximation, and a general approximation. The “thermally thick approximation” was used in this study, which allows for a thermal boundary resistance (TBR) parameter to be introduced into the model. In the configuration with two distinct layers, a TBR parameter is not considered. For these reasons, the thin structure heat transfer model was used in this study.

5.6 Material Properties

Depending on the multiphysics employed in the FEA simulation, a potentially large number of material parameters must be specified. In the current context, the material properties of the various test device components were assigned are summarized in Table 6. The majority of the material properties listed are values for bulk materials, but there are several key distinctions to note. The table contains an entry for both "gold" and "gold NW." Since the objective of performing the simulation work is to determine the thermal conductivity of nanostructures of varying dimensions, a second gold material was established in the model. By creating this second "material," it was possible to examine the unique characteristics of nanostructured material, independent of the gold that constitutes the remainder of the test device. For the "gold NW" material, the thermal conductivity value is listed as "kappa_Au," which will be discussed further in later in this section.

Table 6. Material Parameters for FEA Simulations

Properties	**Materials**				
	Silicon (single crystal, isotropic)	Silicon dioxide	Titanium	Gold	Gold (NW)
Heat Capacity (at constant pressure) [J/kgK]	700	730	522	129	129
Density [kg/m3]	2329	2200	4506	19300	19300
Thermal Conductivity [W/mK]	130	1.4	4.1	317	317

Another important parameter of note is the thermal conductivity of the 5nm titanium layer. The value used in the simulations was 4.1 W/mK, instead of the literature value for titanium of 21.9 W/mK. This is based on data presented by Olson *et al*. comparing O_2 stoichiometry between high vacuum (HV) and ultra-high vacuum (UHV) e-beam evaporation systems. [70] By comparing XPS and XRR data, Olson concluded that titanium deposited using UHV appear to be purely metallic, while the titanium deposited using HV is only 6% metallic, regardless of the rate of deposition. As noted previously, the chamber pressure of the Angstrom evaporator used in this study is typically 3.6×10^{-8} torr, which is considered to be a HV process, as compared to UHV pressures in the 10^{-10} torr regime. Accordingly, the bulk material properties of TiO_2 instead of metallic Ti were used in the model.

The use of TiO_x in the model is further supported by a previous study by the author. X-ray reflectivity (XRR) analysis was performed on a 5nm Ti/50 nm Au film deposited on a silicon wafer with native oxide using the same Angstrom e-beam evaporator with identical process conditions. The reflectivity profile, shown in Figure 49 was generated using a Rigaku Smart Lab X-ray Diffractometer (Tokyo, Japan) with Global Fit software. XRR measures how the reflectance intensity of a thin film changes as the x-ray angle of incidence is changed. Many materials like gold have high reflectivity at low angles, until a critical angle is reached. Above the critical angle, a portion of the incident light is refracted in the surface of the film. The critical angle, or refractive index, is related to the electron density of the material. The reflectivity profile also provides information regarding the film thickness, roughness, and the density contrast. From this profile, the Global Fit software was used to model various film stacks

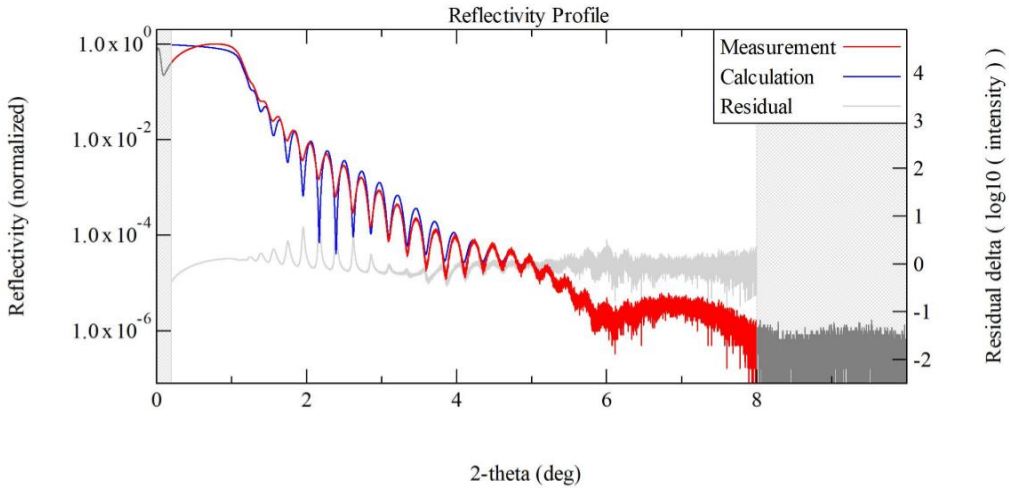


Figure 49. X-ray Reflectivity for 5 nmTi/50 nm Au Film

to best match the reflectivity profile. From this analysis, the best fit was achieved by modeling the 5nm adhesion layer comprised of over 60% TiO_2.

With the materials identified, each material was assigned to components of the model. For the heater and the reference RTD, one layered material stack was defined, with the material and orientation of each layer and interface. A second layered material stack was defined for the sample RTD, inclusive of nanostructure array.

5.7 Heat Transfer and AC/DC Module

Next, the heat transfer in solids module was populated with initial temperatures and constraints for the model. A convective heat flux was applied to the device with a heat transfer coefficient h = 10 W/m^2K and the air temperature set to ambient conditions. The heat transfer coefficient was selected as a standard value for free convection of air. During the electrical testing using the temperature controller, the probe station platen is equipped with forced air cooling using CDA (clean dry air). However, in this study, the air cooling was shut off to eliminate the potential of introducing additional modes of heat

transport in the experimental data. The bottom of the wafer coupon, which contacts with the probe station platen, was designated as a heat sink at ambient temperature.

Within the heat transfer module, four different "solids" were defined in the model: wafer (silicon), oxide (silicon oxide), thin layer 1 (heater and reference RTD sensors), and thin layer 2 (sample RTD with nanostructure array). For the time dependent study, the following constitutive equation is used by the model:

$$\rho C_p \left(\frac{\partial T}{dt}\right) + \rho C_p \boldsymbol{u} \cdot \nabla T + \nabla \cdot (-\kappa \nabla T) = Q \tag{17}$$

where T is temperature, ρ is density, C_p is specific heat, κ is thermal conductivity, $\boldsymbol{u}$ is the translational motion velocity vector of the electrons, and Q is the heat source per unit volume.

In thin layer 1, the "thick layer approximation" was used, with a thermal boundary resistance (TBR) value of 8.01 x 10^{-8} Km^2/W. Room temperature TBR values between metals and dielectrics range between 1 x 10^{-8} and 1 x 10^{-7} m^2K/W depending on the liner/barrier layer used.[116, 117] Olson et al measured TBR values across the Au/TiO_2/substrate deposited under high vacuum, with values ranging from 1.3 x 10^{-8} to 4 x 10^{-9} m^2K/W for various substrate materials, excluding SiO_2. [70] Burzo et al measured the TBR values for $Au/Cr/SiO_2$ ranging from 0.78 x 10^{-8} to 1.15x 10^{-8} m^2K/W.[69] Additional studies conducted by Kading et al for $Au/Cr/SiO_2$ layers measured TBR values of 10 x 10^{-8} m^2K/W. In order to determine a TBR value for the model, a range of TBR values from 1 x 10^{-7} to 1 x 10^{-9} m^2K/W were evaluated in a parametric sweep, and a value of 8.01 x 10^{-8} m^2K/W yielded the best fit.

"Thin layer 2" was used to model the sample RTD, again using the thick film approximation. For the thermal conductivity value, "kappa_Au" served as a fitting

parameter for the parameter estimation step of simulation.

"Electric Current, Single Layer Shell (ecs)" was enabled from the AC/DC module in order to model the applied current to the heater of the test device, using the following constitutive equations for the time dependent study:

$$\nabla_T \cdot (d_s J) = d_s Q_{j,v} \tag{18}$$

$$J = \sigma E + \left(\frac{\partial D}{\partial t}\right) + J_e \tag{19}$$

$$E = -\nabla_T V \tag{20}$$

where Q is the heat source due to the applied electric current, T is temperature, d_s is the thickness of the thin layer (sample RTD with array), D is the electric flux density, J is the current density, E is the electric field strength, and V is voltage.

Within this module, a linearized resistivity method was used to characterize the conductivity σ with the following equation:

$$\sigma = \frac{1}{\rho_o \left(1 + \alpha\left(T - T_{ref}\right)\right)} \tag{21}$$

where ρ is the resistivity, α is the temperature coefficient of resistivity, and T_{ref} is the ambient testing temperature. The inputted resistivity value for the 50 nm devices was derived from numerous literature source for size-dependent, room temperature resistivity of gold, with a value of ρ=37-39 nΩ-m. [102, 118, 119]. For devices fabricated with 100 nm thick gold, the resistivity value used was that of bulk (24.4 nΩ-m). A discussion of device resistivity is provided in Section 6.4. The temperature coefficient of resistance was experimentally determined to be 2.2×10^{-3}/K, consistent with literature findings for nanoscale gold.[106, 119].

The terminal and ground were established on the heater in the model, with an

analytic expression describing current versus time, as shown in Figure 50.

The multiphysics module “Electromagnetic Heating” and “Temperature Coupling” were enabled to characterize the coupled interfaces of heat transfer and electrical currents.

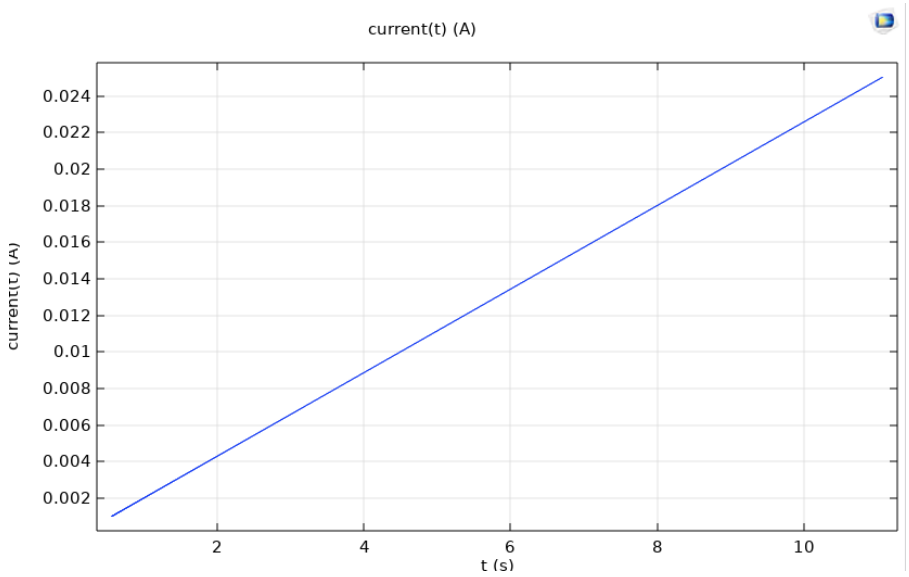


Figure 50. Current vs. Time for COMSOL® Model

5.8 Optimization: Parameter Estimation

With the geometry, materials, and physics of the model established, a time-dependent optimization study was initiated. The time-dependent temperature data of the sample RTD acquired from the electrical testing was inputted into the COMSOL® model as an interpolation function. By using the interpolation function, the experimental data can be incorporated into the model. It is important to note that the model only computes the differences between the simulated and experimental data at the times explicitly stated in the experimental data. [114] Examples of these data sets are presented in Figure 42, Figure 43, and Figure 44. The parameter estimation function performs a least-squares approximation to minimize the difference between the set of experimental data and the

simulated results for the average temperature of the sample RTD. This is an inverse modeling problem where the thermal conductivity of the nanowire array (kappa_Au) is the fitting parameter. The model estimates the value of kappa_Au so that the simulated results best match the experimental results. Within COMSOL® Multiphysics, there are several different optimization algorithms available to perform the parameter estimation. In this study, the Boundary Optimization by Quadratic Approximation (BOBYQA) method was selected, as the optimization solvers of the other available algorithms did not readily converge with this model. This is not uncommon, as some of the optimization algorithms require an upper and lower bound for the parameter which often resulted in lack of convergence. The results analysis from the FEA modeling will be presented in Chapter 6.

5.9 Summary of Chapter

In this chapter, a description of the SEM characterization work on the gold nanostructures and devices was described, with a grain size analysis for the two deposition thickness levels. The various nanowire array configuration were presented and the thermal response of the different configurations was compared. The FEA simulation was also presented in this chapter, with attention to the approach used to the mesh the geometry. The various COMSOL® modules that were used in the simulation work were discussed along with the material properties and boundary conditions. The selection of the TBR parameters was also presented. Finally, the process for determining the thermal conductivity from the experimental data was discussed.

6. DISCUSSION OF RESULTS

Time-dependent FEA simulations were performed on a series of test devices at 50 nm and 100 nm deposition thickness levels with varying nanostructure array dimensions at both room temperature (25 - 30°C) and 100°C ambient conditions. In addition to the time-dependent study, the FEA simulations included an optimization step to perform a parameter estimation of the thermal conductivity for each nanostructure array. In this section, the agreement of the simulated results with the experimental data will be discussed as well as the thermal conductivity values obtained for each condition. Comparisons with results found in literature will be presented and possible mechanisms for the observed behavior will be explored.

Like most predictive models, there are several underlying assumptions. In this case, it is assumed that both the current distribution and mass distribution is uniform. Further, it is assumed that the heat capacity is constant, independent of temperature and that thermal isolation is uniform. The ambient temperature is also assumed to be constant. Material properties are assumed to be isotropic.

6.1 Comparison of Nanowire/Nanofilm Widths and Thickness

Thermal conductivity, commonly regarded as an intensive material property, has a strong dimensional dependency at the nanoscale. In fact, thermal conductivity reveals the processes that are occurring at the fundamental scale of the energy carriers.[55] The size effects of nanoscale structures has been a topic of intense research for many years.[68, 120] In this study, a series of test devices was fabricated that represents a range of nanowire/nanostructure widths, from 74 nm to 720 nm, at both 50 nm and 100 nm deposition thickness levels.

As noted in Section 4.7, the gold heater of the test device was found to withstand a maximum current density of 3.7 x 10^{11} A/m^2 prior to failure. For the 100 nm deposition thickness, a current sweep was performed with a maximum drive current of 25 mA in order to stay below the current density limit, while a maximum heater drive current of 15 mA was used for the 50 nm thick devices.

Figure 51 illustrates the sample and reference RTD thermal response to a current sweep (0-15 mA) for a 50 nm thick sample with a 135nm width nanowire array at room temperature. As the heater current increases, a measurable difference in temperature is realized between the sample and reference RTDs. The error bars on the experimental data

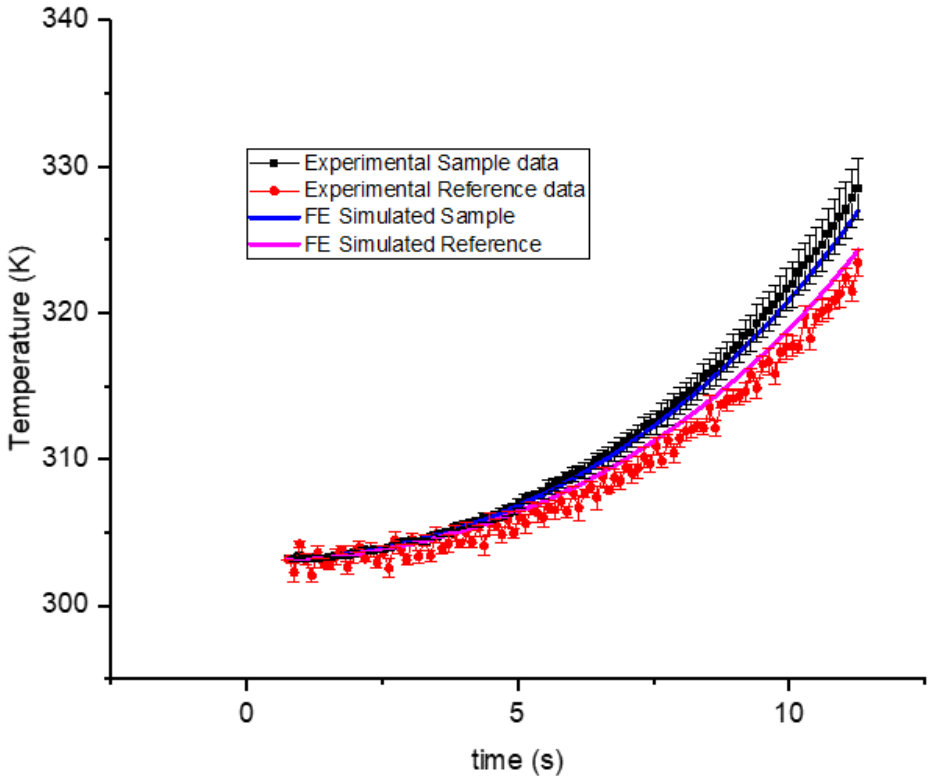


Figure 51. Comparison of Experimental and Simulated Thermal Response.
50 nm thickness, 135 nm width wire array, at 298K

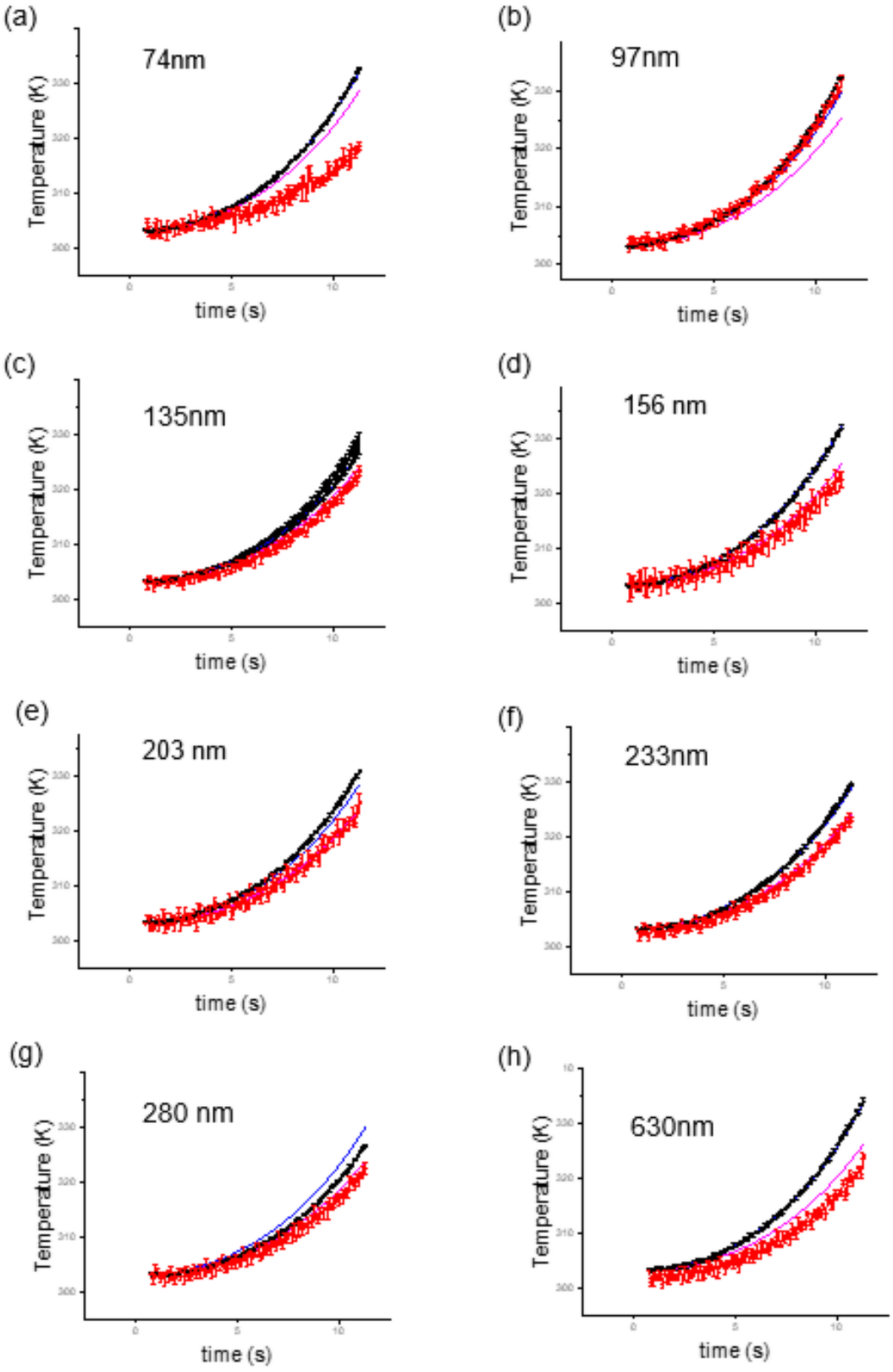


Figure 52. Experimental vs. Simulated Results, 50 nm thickness at 298K.

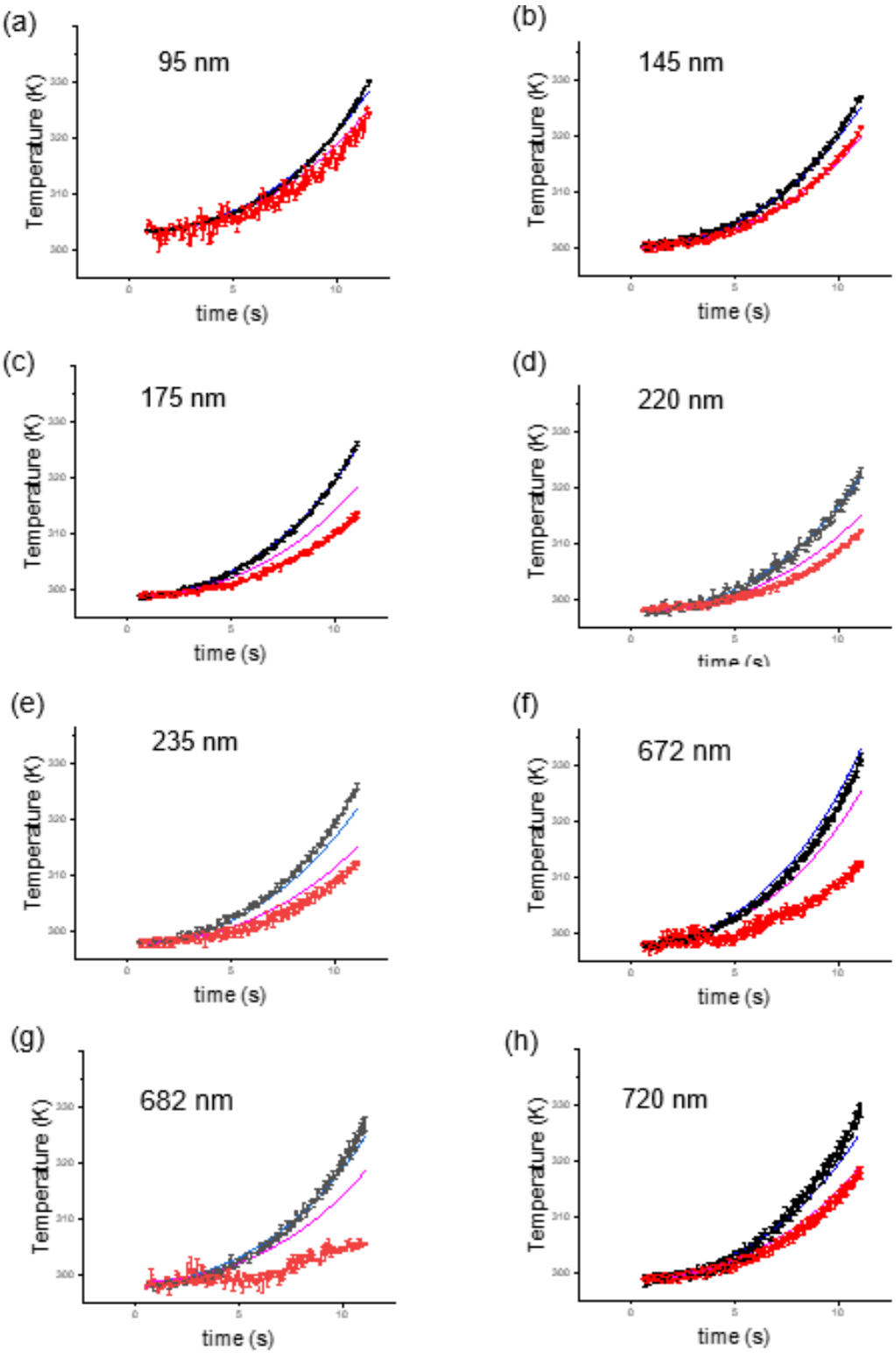


Figure 53. Experimental vs. Simulated Results for 100 nm Thickness at 298K.

were derived from the standard deviation of data from multiple current sweeps for a given device. The FEA simulated results, designated as “FE Simulated Sample” and “FE Simulated Reference,” is also shown in the figure. In this case, there is excellent agreement between the experimental data and the simulated response for both the sample and reference RTDs. Through the least-squares optimization in COMSOL®, a thermal conductivity value for the 135nm nanowires (50 nm thickness) was determined to be 118 W/mK, which is considerably lower than the 317 W/mK for bulk gold. A representative sampling of the experimental and FEA simulations for both the 50 nm and 100 nm thickness devices at room temperature is shown in Figure 52 and Figure 53, respectively.

In most cases, the FEA simulated response for the sample RTD is in good agreement with the experimental data, but the experimental reference RTD data was often considerably lower in temperature than the response predicted by the model. The model compares the measured temperatures of the sample RTD to the simulated temperature of the sample RTD. In the course of the simulation, the thermal conductivity is varied using a least squares approximation to arrive at the best fit to the data. Good agreement between the experimental and simulated results for the sample RTD is the result of numerous iterations to arrive at a suitable thermal conductivity value, while agreement between the experimental and simulated results for the reference RTD is desired, but not critical to the study. The simulated responses take into account the convective heat transfer occurring through the substrate from the heater to the RTDs. On the sample RTD, greater heat transport is promoted by the presence of the nanowire/nanofilm array, while the reference RTD response is purely due to heat

conduction through the oxide substrate. In summary, it is the sample RTD measurement that is critical for obtaining thermal conductivity of nanowires and nanofilms.

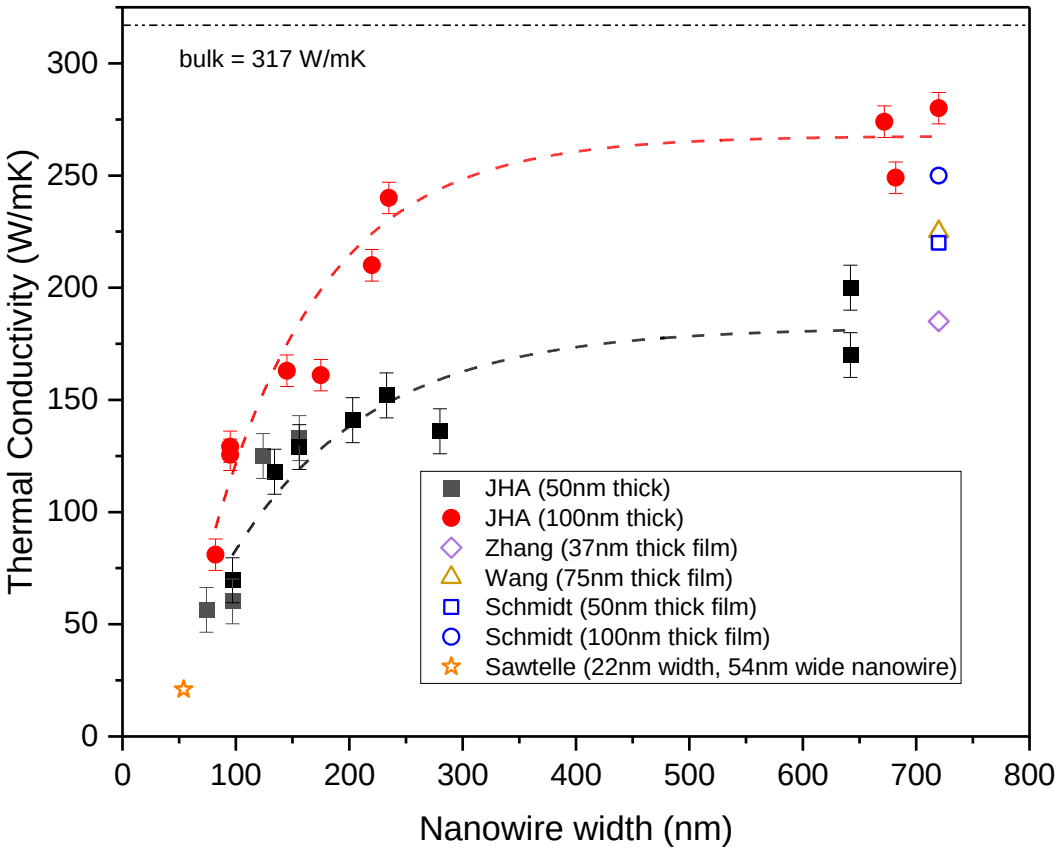


Figure 54. Thermal Conductivity vs. Nanowire Width for 50 nm and 100 nm thickness.
with literature data at room temperature
(note: the data line serves as a guide to the eye)

Presented in Figure 54 is the principle outcome of this research: the impact of nanoscale dimension on the thermal conductivity of gold based on *direct* studies. Both the 50 nm and 100 nm thick conditions demonstrate increasing thermal conductivity with increasing nanowire width. For both device thickness levels, the thermal conductivity of the lower dimension arrays is shown to initially exhibit a steep increase with increasing nanowire width, but then appear to level off at higher nanowire widths. Overall, the

100 nm thick conditions possessed higher thermal conductivity values than the 50 nm thick conditions.

For both the 50 nm and 100 nm thick devices, several device geometries were replicated. For example, several devices were fabricated with 100 nm (± 5nm) width wires for a given thickness. Simulations were performed for each current sweep on the replicated devices to determine a thermal conductivity value. In the case of the cited example, this represents six thermal conductivity measurements for the 100 nm width wire condition. The error bars indicate two standard deviations from the measurements. Similar to the results of Schmidt *et al*., larger uncertainties were generated for the 50 nm thick devices as compared to the 100 nm thick devices. This may be due to the fact that the thinner films transport less heat, so the measurement may be less sensitive.[66] In other words, the method relies on heat conduction by the samples and when that is reduced, their importance is commensurately reduced. Extending this to lower thickness values would result in a temperature field that is independent of sample and, therefore, provides increasingly compromised estimate of the desired measurement.

When the dimensions of the nanowire are on the same order of the electron mean free path, the thermal conductivity has been shown to drop by roughly half the bulk value [68]. For the 50 nm (±5 nm) thickness, the thermal conductivity was found to be approximately 63% of the bulk thermal conductivity value of 317 W/mK for the nanofilm configurations tested. In the case of the100 nm (±5 nm) thick nanofilms, the thermal conductivity was determined to be 88% of bulk values. Since the minimum dimension of the devices tested are larger than the 37.3 nm MFP for gold [26], the percentage reduction in thermal conductivity seen is this study seems reasonable.

In addition to experimental data, Figure 54 also includes data from other researchers, as outlined in Table 7. There is limited availability of direct measurements of gold nanowires and films due to the inherent difficulty of the measurement itself. The literature data included in this study are results from both nanowires and nanofilms. The higher width dimension conditions (>600 nm) in this study are assumed to be comparable to a nanofilm, considering the geometry of the devices since the width dimension approaches or exceeds the thickness dimension. This assumption is confirmed by the agreement of the nanofilm data presented by Schmidt *et al.* for 50 nm and 100 nm thickness and the results of the measured thermal conductivities for the nanostructure widths larger than 600 nm. Studies by Langer et al. also demonstrate similar behavior in the thickness dependency of gold nanofilms. [121]

Table 7. Literature Sources for Figure 54

Data Source	**Conditions**
Zhang, *et al.* [122]	37 nm thick gold film, suspended, direct current heating method, ambient temperature = 300K (temperature range for study = 80-300K)
Wang *et al*. [109]	76 nm thick gold film, supported on Si/SiO_2 substrate, measurement taken with spring contact four probe device, ambient temperature = 295K (temperature range for study = 3-295K)
Schmidt, *et al*. [66]	50 nm thick gold film, sputtered on fused silica, measured using FDTR, ambient temperature = 295K for all testing
Schmidt, *et al.* [66]	100 nm thick gold film, sputtered on fused silica, measured using FDTR, ambient temperature = 295K for all testing
Sawtelle, *et al.* [4]	22 nm thick 54nm wide gold nanowires, supported on SiO_2, direct current heating method, ambient Temperature = 260K (temperature range for study = 95-260K)

The results demonstrate the significant impact of both deposition thickness and nanowire width on the resultant thermal conductivity. Additionally, there is excellent agreement between all experimental results. This is especially satisfying since these results show agreement despite the vast differences in experimental methods.

Zhang *et al*. conducted temperature-dependent tests on suspended gold nanofilms of 21-37nm thick with a direct current heating method under vacuum. Both electrical and thermal conductivities were found to be greatly reduced as compared to bulk values, with a more prominent reduction as the temperature is reduced from 300K to 80K. The temperature behavior is attributed to the increase of the electron MFP with decreased temperature, so that the size effects are more pronounced. The selection of the film thickness was such that the grain size and film thickness are comparable to the electron MFP at room temperature. Both surface and grain boundary scattering are believed to cause the reduction of electronic and thermal conductivities. To understand this behavior, the authors considered the approach of Mayadas and Shatzkes [63] to incorporate grain boundary and external scattering as boundary conditions to solve the Boltzmann equation (BTE). The decrease in electrical conductivity values of the nanofilms relative to bulk values were considerably larger than the decrease observed in the thermal conductivity values measured, which is a violation of the W-F law. The Lorenz number calculated from the nanofilm data in this study was approximately 7.0×10^{-8} $W\Omega/K^2$, which is considerably larger than the value predicted for metals by the W-F law of 2.44×10^{-8} $W\Omega/K^2$.

Wang *et al*. conducted temperature-dependent electrical and thermal conductivity tests on 53 nm and 76 nm thick gold nanofilms supported on a Si/SiO_2 substrate using 4-

point contact direct current heating under vacuum. Similar to the Zhang *et al.* results, the researchers in this study observed breakdown of the W-F Law, with a significant increase of the Lorenz number for the nanofilm tested. Based on the observed temperature behavior, the authors concluded that phonon thermal conduction is "not negligible." Thermal conductivity values for the 76 nm nanofilm condition in the Wang *et al*. study were found to be in between the values of the 50 nm and 100 nm thick conditions in the present study.

Schmidt *et al*. utilized FDTR on gold and aluminum films supported on a fused silica substrate to measure the thermal conductivity, while electrical conductivity values were obtained using Hall measurements on van der Pauw devices. Comparisons were made between the direct thermal conductivity measurements using FDTR and W-F Law predictions using the measured electrical conductivity. The results indicated generally good agreement between the FDTR-generated thermal conductivity data and the W-F predicted values, except for the low film thickness of 22 nm, where the measured values was 40% greater than the predicted value. This discrepancy is believed to be related to grain boundary scattering, which has a greater effect on electrical conductivity than thermal conductivity at low dimensions. Another possible explanation is due to the inherent roughness of the 20 nm film as compared to greater film thicknesses, which may enhance both electron and phonon scattering. Finally, the researchers experienced difficulty making good electrical contact with the soft, thin gold film. As noted previously, the 50 nm and 100 nm thermal conductivity values from the Schmidt *et al.* study agree well with the experimental data in the present study.

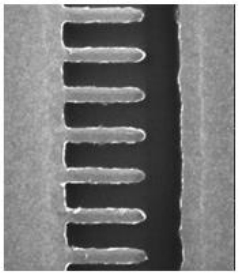
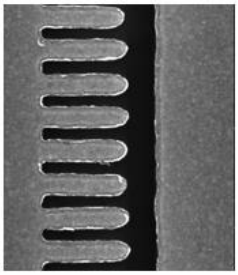
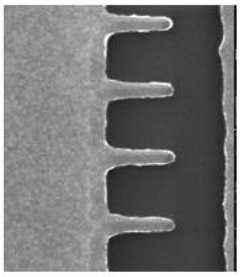
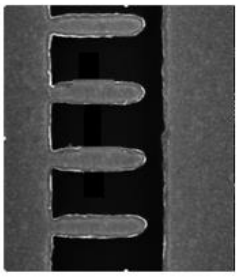
Sawtelle, *et al.* represents one of the few data sources found in literature for

measuring the temperature-dependent thermal conductivity of gold nanowires using direct current. In this study, 22 nm thick gold nanowires varying in widths from 20 to 60 nm were fabricated on a very thin layer (22 nm) of SiO_2 with a thick Si handle. Although their study involved nanowires of much lower dimensions than considered in this study, the results support the trend reported here where reduced nanowire widths resulted in depressed thermal and electrical conductivity values. This reduction can be attributed to increased structural scattering with decreased widths. The data does not agree with predicted W-F results, but, unlike the other researchers, Sawtelle et al. found Lorenz numbers were substantially lower than bulk values, especially for the lower dimension nanowires. The authors consider several potential mechanisms for this behavior, including low frequency vibrations within the ultra-thin gold layer causing thermal annealing, and substrate heat-sinking.

6.2 Comparison of Pitch

In some of the lower In some of the lower dimension (< 150 nm nanowire width) test devices, the nanowire arrays were designed with a 1:1 pitch or a 1:2 pitch for a given nanowire width, as discussed previously in Section 5.3 and shown in Table 8. The narrow pitch conditions were included in the study with the intent of achieving a significant, measurable temperature difference between the sample RTD and the reference RTD. The narrow pitch configuration was challenging from a fabrication standpoint. The successful lift-off of the material between the nanowires required optimal dosage during the e-beam lithography process and a lift-off methodology that was successful in removing the

Table 8. Two Pitches for Two Nanowire Widths

Pitch	97 nm width	156 nm width
Narrow	 Fill factor = 22.5%	 Fill factor = 50.1%
Wide	 Fill factor = 11.7%	 Fill factor = 25.5%

material between the wires, but not too aggressive to damage the wires and device.

Also included in is the “fill factor” for the four pitch configurations. As noted in Section 5.3, the fill factor refers to the ratio of the area of the gap between the heater and sample RTD that is occupied by the nanostructure array. These fill factors were determined using SEM images. For both examples shown in the table, the narrow pitch configuration has twice the fill factor of the comparable wide pitch configuration. Intuitively, one would expect that a device with a higher fill factor should result in a higher sample RTD temperature, since an increase in metal volume in the gap promotes heat transfer between the heater and sample RTD.

The temperature difference between the sample and reference RTDs for the different pitch configurations and fill factors shown in Figure 55. Each representative test

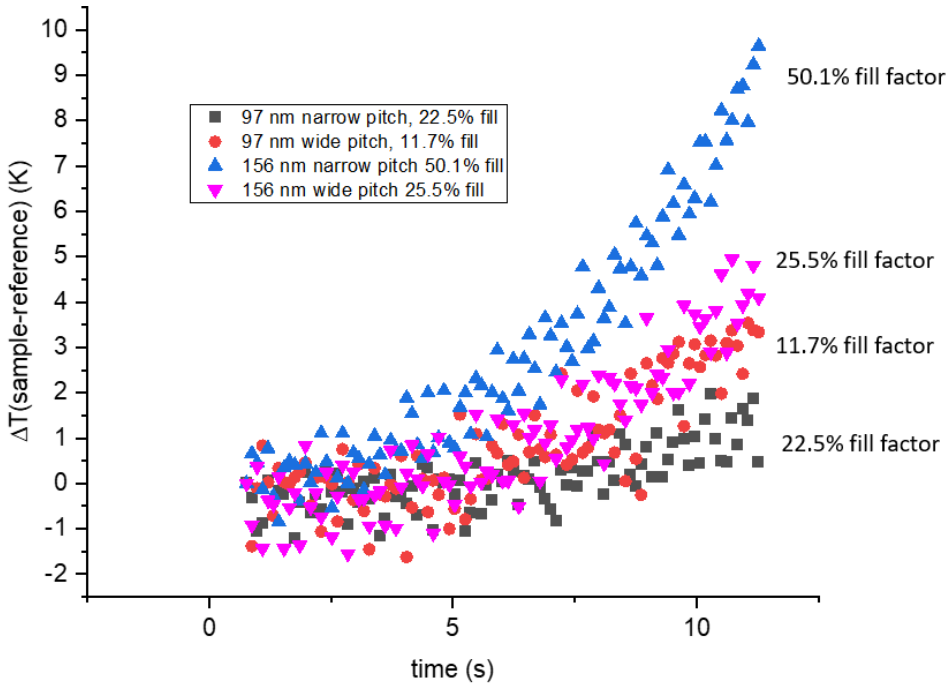


Figure 55. Effect of Pitch and Fill Factor on the Temperature Difference Between RTDs. (50 nm deposition thickness. Error bars are not included in graph for clarity purposes. Testing conducted at room temperature)

device was interrogated at room temperature conditions with a heater current sweep of 0 to 15 mA. The highest fill factor of 50.1% (156 nm, narrow pitch) resulted in the largest differences between the sample and reference RTDs. The remaining devices exhibited moderate temperature increases throughout the current sweep. While there is considerable variability in the data, it appears a trend exists, where the 156 nm conditions result in a greater temperature increase over the current sweep as compared to the 97nn conditions. This is due to the higher thermal conductivity of the wider nanowire widths, where the measured thermal conductivity of the 156 nm configurations range between 129- 133 W/mK (±7 W/mK), while the thermal conductivity of the 97 nm width conditions was determined to be 60-69 W/mK (±7 W/mK). Unexpected is the higher temperature increases obtained thermal conductivity and higher than expected TBR for the latter nanowire array.

The sample RTD temperature data was used in FEA models to perform a for the wide pitch 97 nm condition with a 11.7% fill factor than the narrow pitch counterpart with higher fill factor of 22.5% Possible reasons for this include lower parameter estimation for the determination of thermal conductivity for each nanowire width/pitch combination. The precise geometry of each individual test device is included in the simulations, so the predicted thermal conductivity is agnostic to the irregularities among and between test devices.

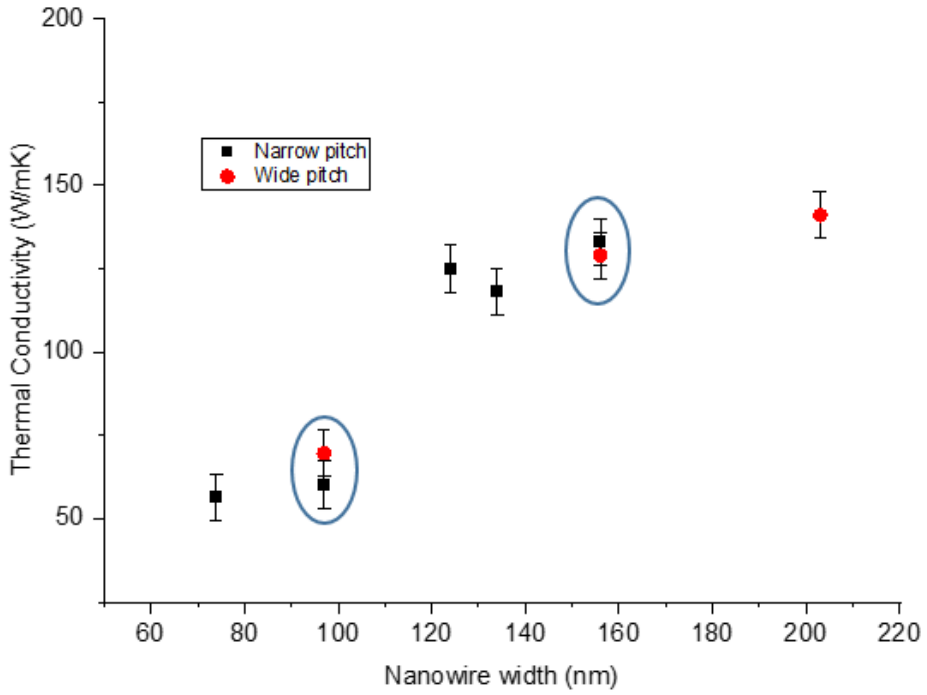


Figure 56. Thermal Conductivity vs. Nanowire Width for Different Pitches.
50 nm Testing conducted at room temperature

The predicted thermal conductivity values for narrow and wide pitch arrays for 50 nm deposition thickness is shown in Figure 56, with the 97 nm width and 156 nm conditions circled. Thermal conductivity values are shown to increase with increasing nanowire width, where the thermal conductivity of the 156 nm conditions are shown to

be significantly higher than the 95 nm conditions. Further, the pitch, along with the associated difference in the number of nanowires in the array, does not appear to have statistically significant impact on the thermal conductivity values determined in the simulations.

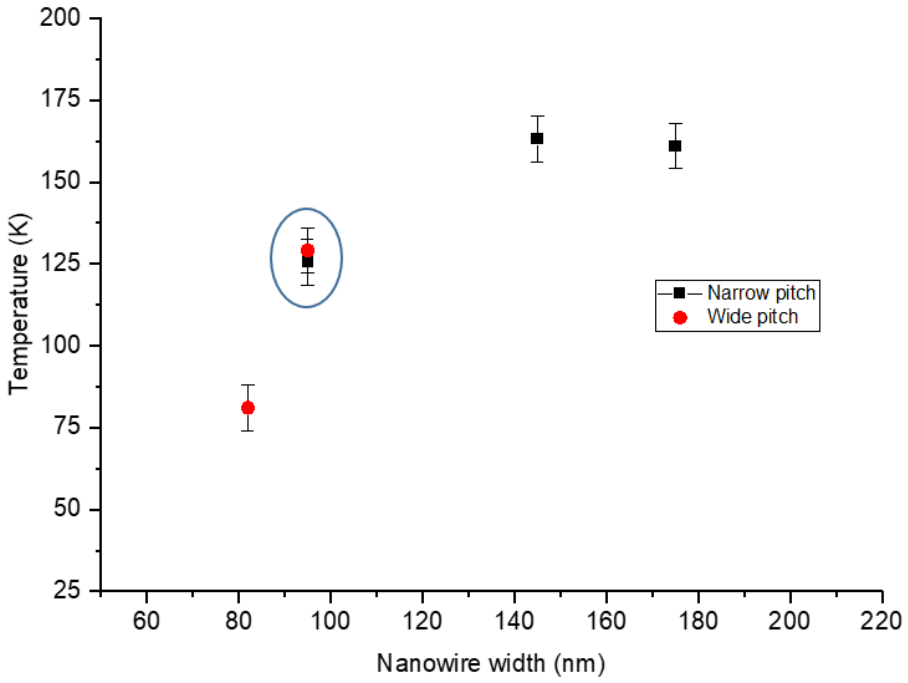


Figure 57. Comparison of Narrow and Wide Pitch.
100 nm thickness at room temperature

A similar response was found in the 100 nm thickness condition for 97 nm nanowire width. As seen in Figure 57, the narrow and wide pitch configurations for the 97 nm nanowire width (circled) had an indiscernible impact on the thermal conductivity values generated in the simulations.

These results suggest that the simulation approach developed in this study provides a robust method to determine thermal conductivity of a given nanowire width, regardless of pitch or number of nanowires in the device. The ability to use wider pitch

configurations, which are easier to fabricate than their narrow pitch counter parts, is a useful outcome of this study.

6.3 Temperature Dependence of Nanoscale Thermal Conductivity

Testing was also conducted at 100°C to obtain results approximating the standard operating conditions of an electronic (logic) device [18]. Temperature control was achieved through the heated platen of the electrical probe station which was allowed to equilibrate for at least 10 min prior to testing. A comparison of the experimental data to the simulated response at 100°C ambient temperature is shown in Figure 58. Figure 60 and Figure 61 present a comparison between the experimental and simulated results for the 50 nm and 100 nm thick devices, respectively. The legend for each graph is identical to that shown in Figure 58. The 50 nm devices were heated by a current sweep of 0 to 15 mA, while the 100 nm devices were heated by a current sweep of 0 to 25 mA. Similar to the room temperature results, excellent agreement was achieved for the various device geometries. While 100°C represents a relatively modest temperature increase temperature increase, researchers found that the bulk thermal conductivity of gold decreases slightly with an increase of 300K to 400K, from 317 W/mK to 311 W/mK [86, 123], a 2% decrease.

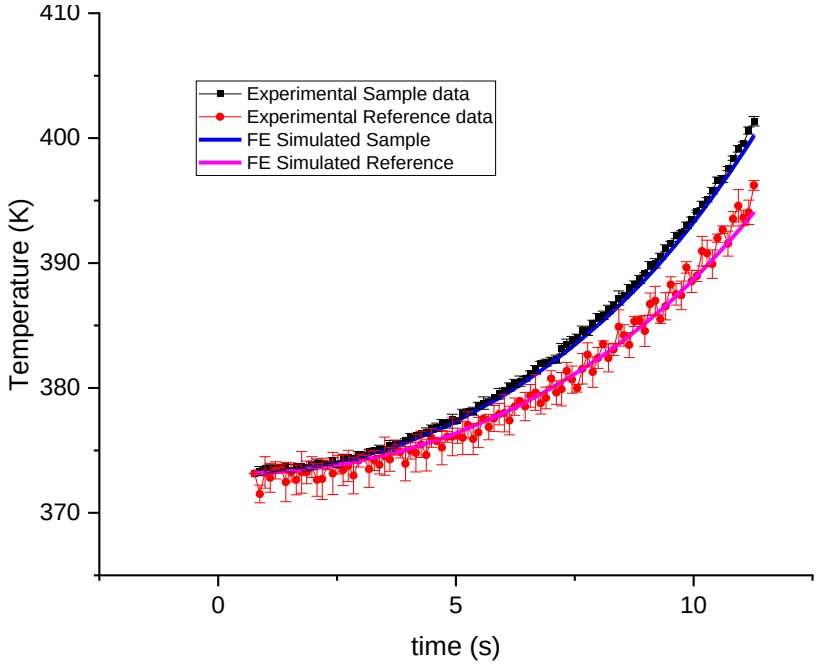


Figure 58. Experimental vs. Simulated Temperature Response at 100C.
287nm width nanowire array, 50 nm thickness

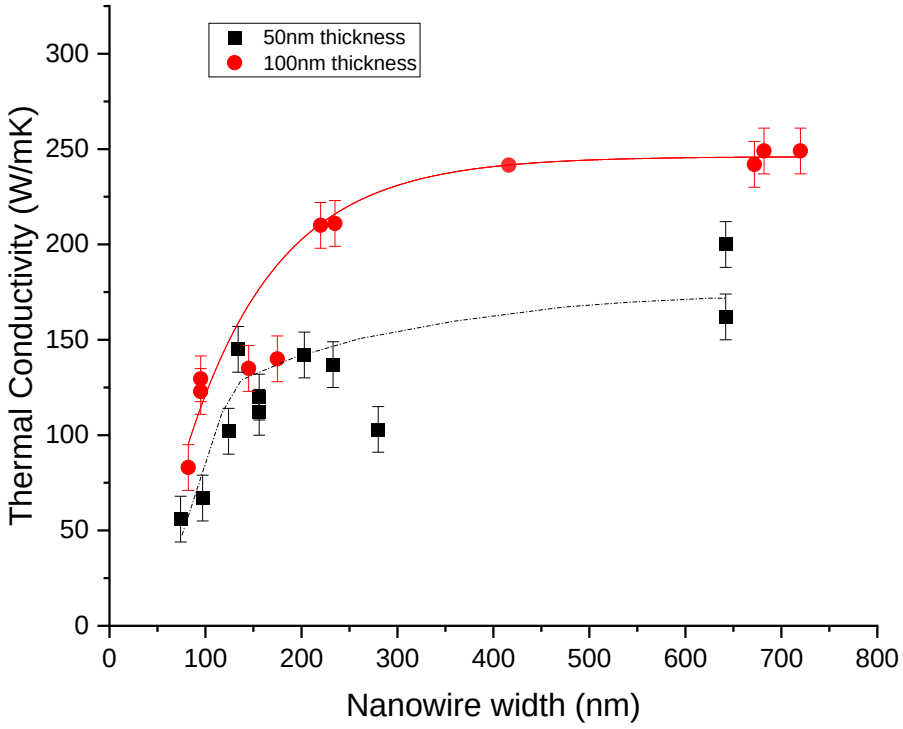


Figure 59. Thermal Conductivity vs. Nanowire Width at 100C.
(bulk gold = 311 W/mK) (note: the data line serves as a guide to the eye)

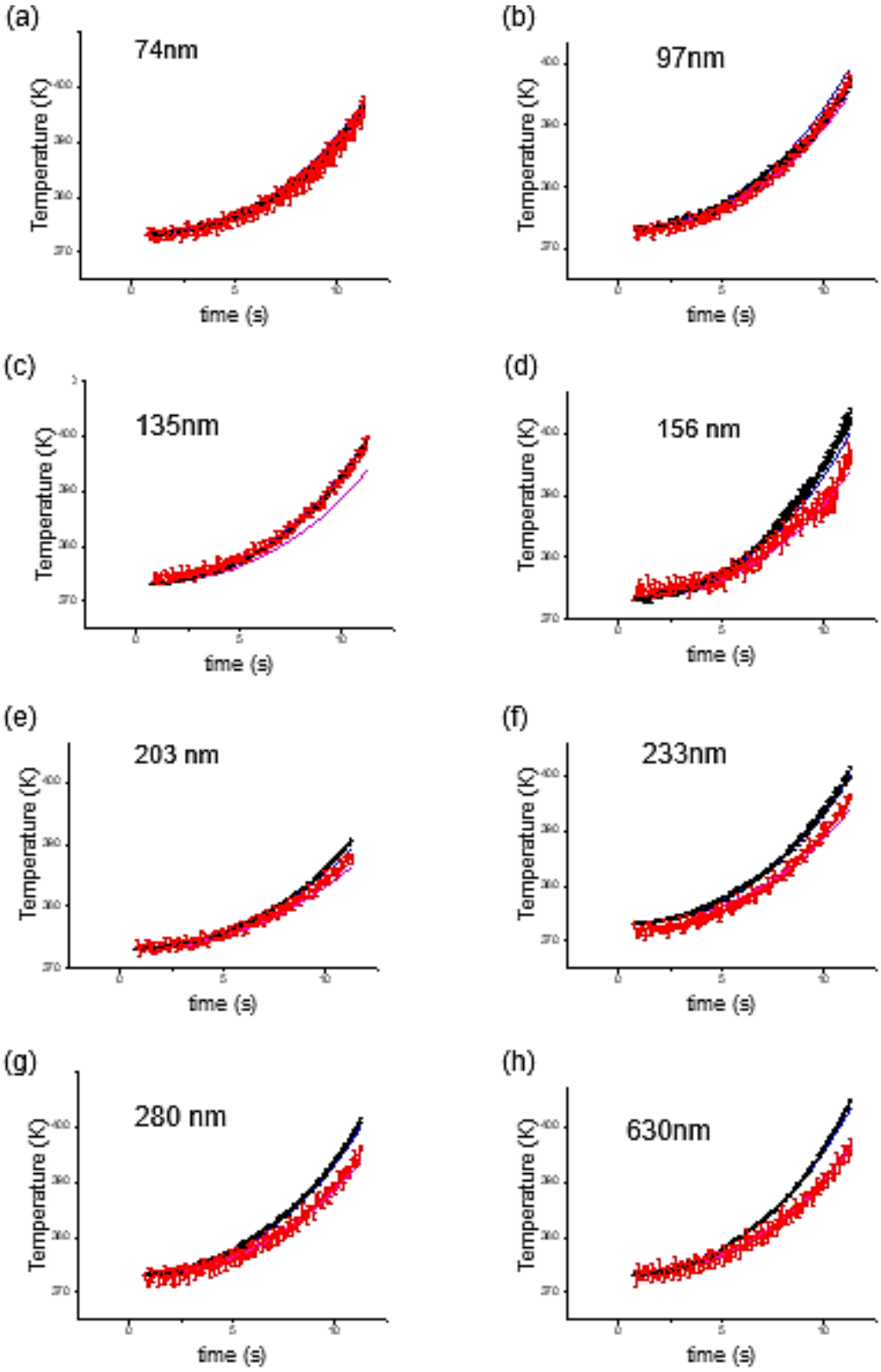


Figure 60. Experimental Data vs. Simulated, 50 nm thickness at 100C.

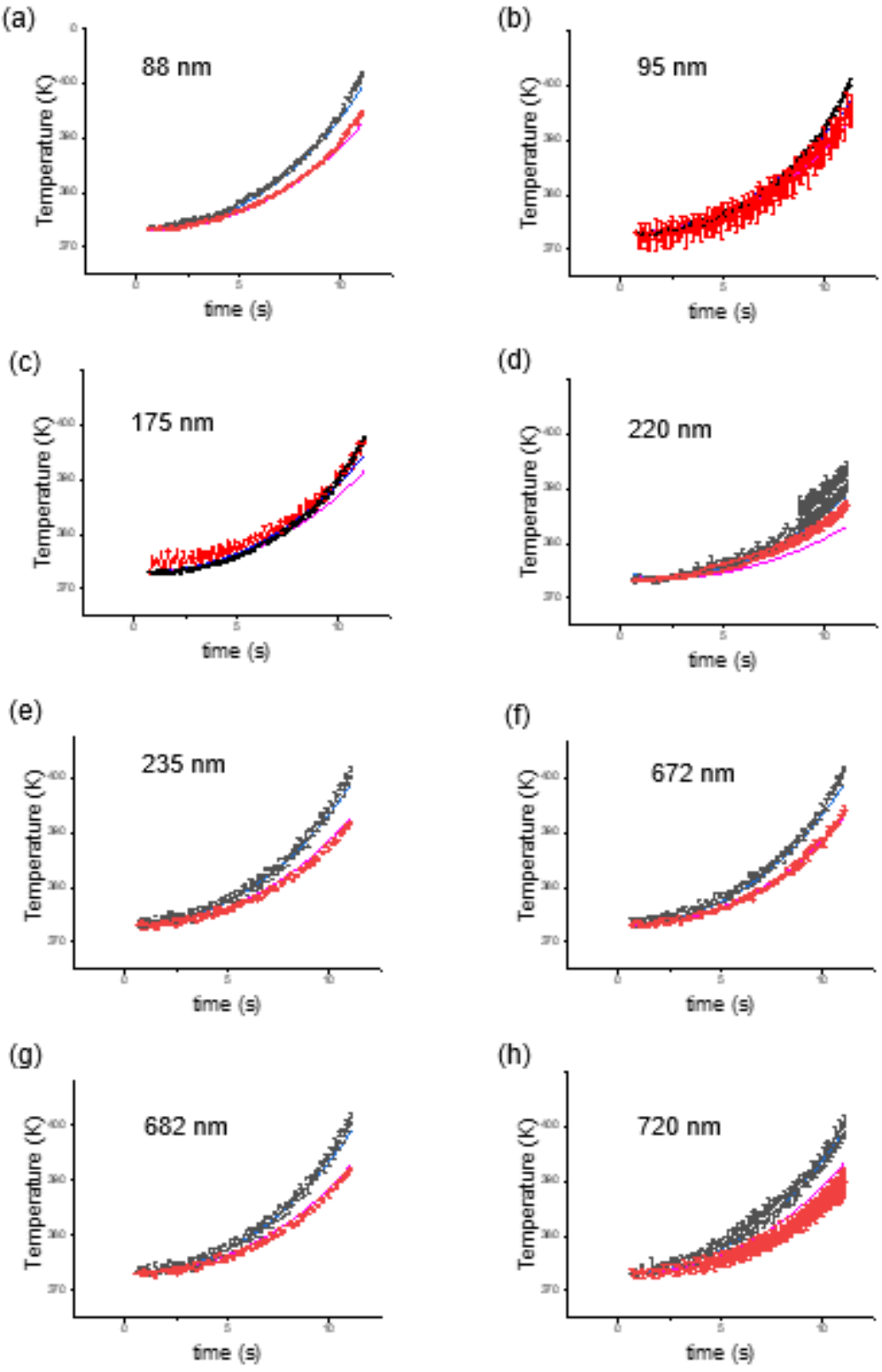


Figure 61. Experimental data vs. Simulated, 100 nm thickness at 100C.

The effect of deposition thickness on thermal conductivity at elevated temperature is shown in Figure 59. Similar to the room temperature testing response, both the 50 nm and 100 nm thick devices show increasing thermal conductivity with increasing wire width, with a leveling off as the width approaches film thickness. The thermal conductivity of the 100 nm nanofilm condition was approximately 80% of the bulk value at 100°C, while the 50 nm nanofilm was 60% of bulk.

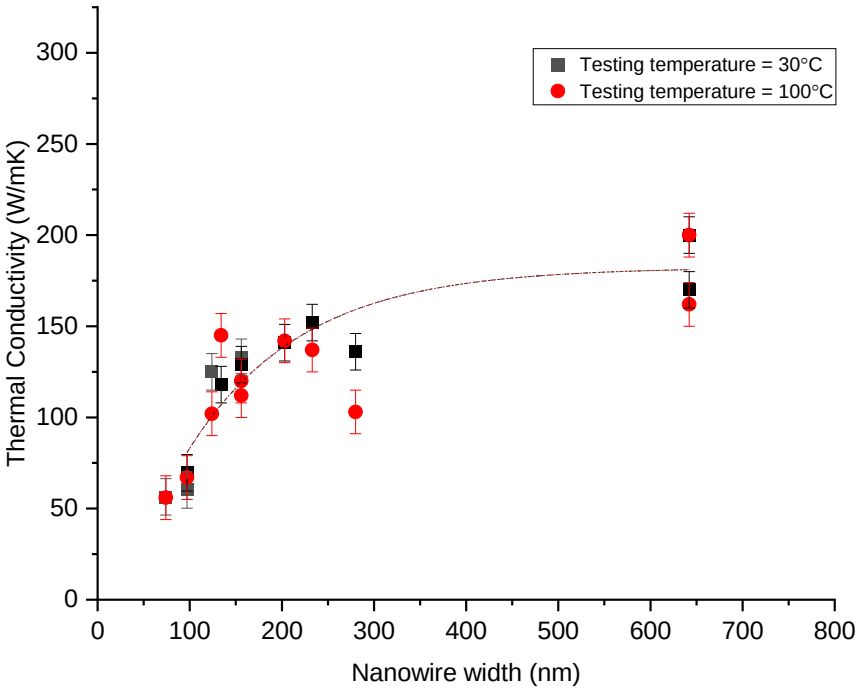


Figure 62. Temperature Dependency of Thermal Conductivity, 50 nm thick.
(note: the data line serves as a guide to the eye)

A comparison of thermal conductivity values for 50 nm thick conditions at room temperature and 100°C is shown in Figure 62. It is apparent that the response is not consistent throughout the nanowire width range evaluated. Conversely, the thermal

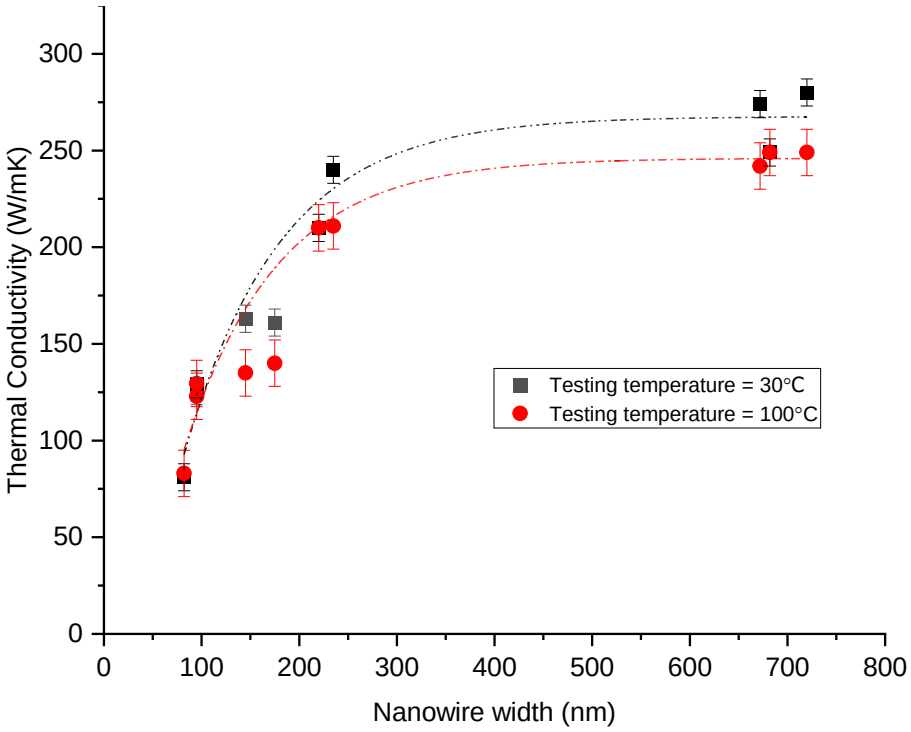


Figure 63. Temperature Dependency of Thermal Conductivity, 100 nm thick.
(note: the data line serves as a guide to the eye)

conductivity values for the 100 nm conditions, as shown in Figure 63. The figure illustrates a significant difference between the room temperature and 100°C conditions. For the 100 nm conditions, the elevated testing temperatures yield lower thermal conductivity values than their room temperature counterparts, particularly at higher nanowire widths.

To gain a better understanding of the nanowire response at elevated temperature, the ratio of the nanowire thermal conductivity (k_{nw}) to the bulk thermal conductivity (k_{bulk}) room temperature and 100°C conditions were plotted against the range of nanowire width considered for both 50 nm and 100 nm devices.

When considering this data, it is important to remember that devices were initially tested at room temperature and then the same device was heated to 100°C and tested

again. This means that the specific device that generated the room temperature data also generated the 100°C data. With this in mind, by considering the 50 nm device data, as shown in Figure 64, it is apparent that there are several instances (circles) where data points overlap for a given nanowire width. This suggests that the measured thermal conductivity at room temperaature experienced the same degree of reduction relative to bulk values as the measurements at 100°C.

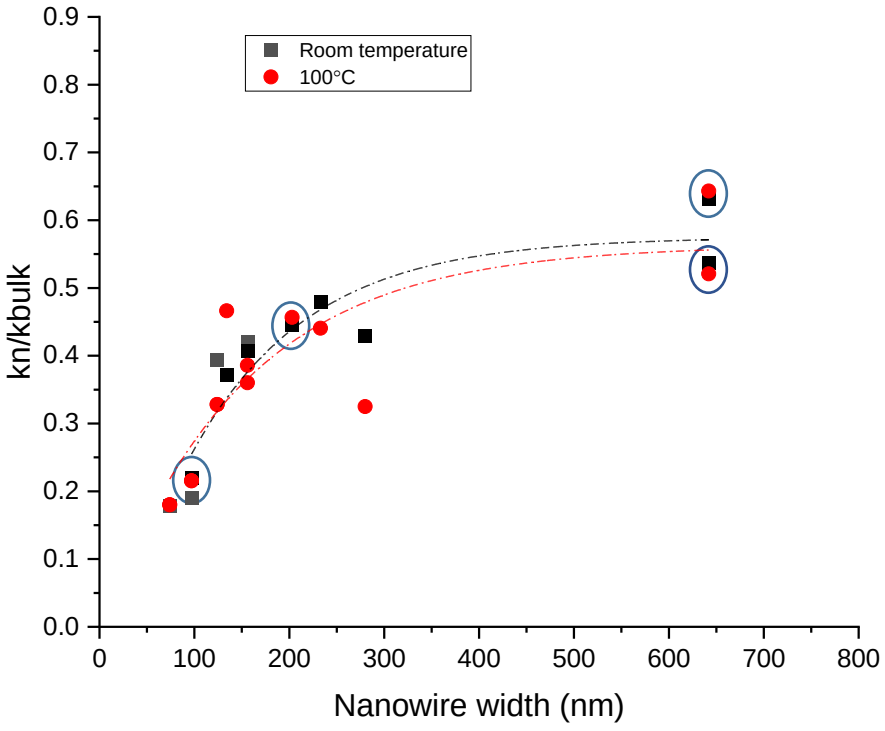


Figure 64. Ratio of Nanowire/film Thermal Conductivity to Bulk, 50 nm thick.
at room temperature and 100°C.

Similarly, the ratio of nanowire thermal conductivity to bulk thermal conductivity for the 100 nm conditions is shown in Figure 65. Again, there are several instances where the data points overlap for the room temperature and 100°C conditions (circled in figure). then diverge at higher nanowire dimensions.

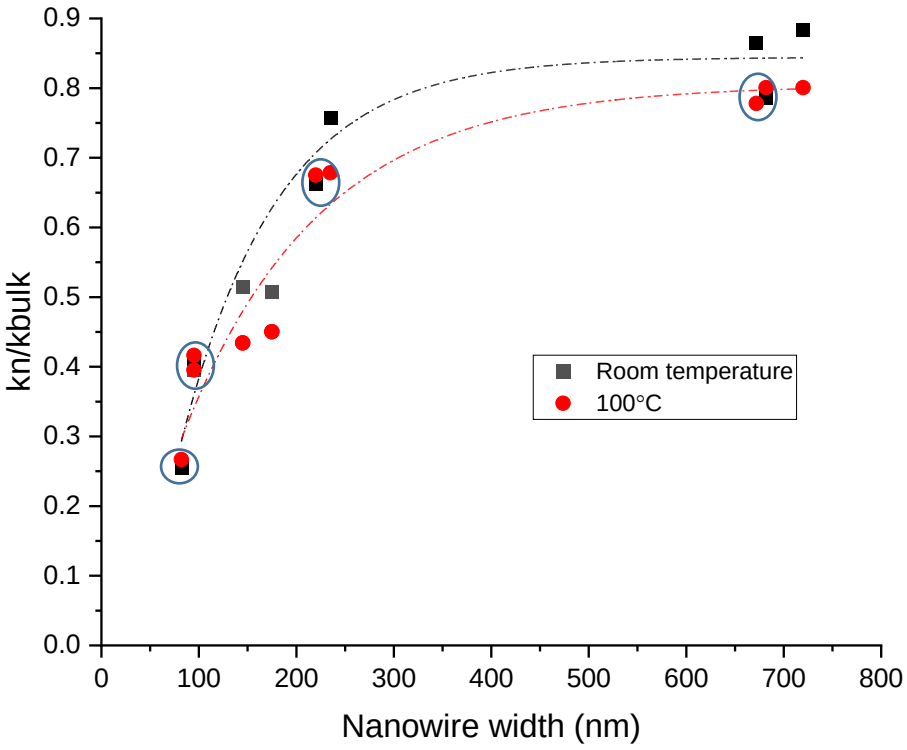


Figure 65. Ratio of Nanowire/film Thermal Conductivity to Bulk, 100 nm thick. at Room Temperature and 100°C

The scatter of the resistance data was also increased during elevated temperature testing, as evidenced by the larger error bars of the 100°C conditions, as shown in Figure 62 and Figure 63. These testing factors may be exaggerated in the 50 nm conditions, as a possible explanation for the inconsistency of the thermal conductivity values at elevated temperatures. Scattering mechanisms depend, in part, on the morphology of the material, and the 50 nm conditions possess a finer grain structure and an overall higher roughness level than the 100 nm conditions, as discussed in Section 5.2.

Curve fitting of both the room temperature experimental thermal conductivity data, shown in Figure 54 and the 100°C data shown in Figure 59 provides some interesting insights. The fit is an exponential decay for thermal conductivity as a function

of nanowire width, shown as

$$\kappa(w) = \kappa_{\infty}(1 - e^{-\frac{w}{\delta}}) \tag{22}$$

where κ_{∞}corresponds to the asymptotic thermal conductivities for the respective thickness levels, w is the nanowire width, and δ is suggestive of a length scale that imposes a limit on the heat carriers. Table 9 presents the fitting parameters for the curves shown in Figure 54 for room temperature measurements, and for 100°C measurements. Specifically, the δ value is several times greater than both the MFP of gold (37.7 nm). It is also larger than the average grain sizes of the 50 nm and 100 nm thickness levels, 27 nm and 35 nm, respectively, from SEM analysis.

Table 9. Fitting Parameters for Figure 54 & Figure 59

	Room Temperature		**100C**	
Thickness (nm)	$\boldsymbol{\kappa_{\infty}}$ (W/mK)	**δ** (nm)	$\boldsymbol{\kappa_{\infty}}$ (W/mK)	**δ** (nm)
50	183 ±15	153 ±30	170 ± 26	155 ± 59
100	274 ±12	147 ±16	240 ± 15	147 ±23

It is important to note that the error associated with these parameters is considerable. Since both thickness levels were fabricated via e-beam evaporation, perhaps the δ parameter is related to the columnar morphology that the deposition process promotes, as shown in Figure 38. Another possible explanation may be related to the adhesion layer, common to both the 50 nm and 100 nm metallizations. Regardless, it is interesting that the δ parameter is consistent for both thickness levels and for both testing temperature conditions.

In summary, the thermal conductivity data demonstates a dependency with temperature which is consistent with a reduction in thermal conductivity of bulk gold. Moreover, the same dependency on thickness and nanowire width was observed. While this is not surprising, little data exists in literature from direct measurements.

6.4 Size Effects and Electrical Resistivity

One contributing factor for the disparity between nanoscale electrical resistivity and thermal conductivity values and bulk values is known as "size effects," as reported previously by numerous researchers. [61, 68, 102, 120-122, 124, 125] The combination of the polycrystalline gold grain sizes along with low dimensions of the nanowires provides numerous thermal barriers and scattering sites for heat carriers, causing a depression in both electrical resistivity and thermal conductivity values.

One approach used to measure the electrical resistivity of the nanowires was the creation of "dogbone" devices, shown in Figure 66. A wire of 10 μm length was

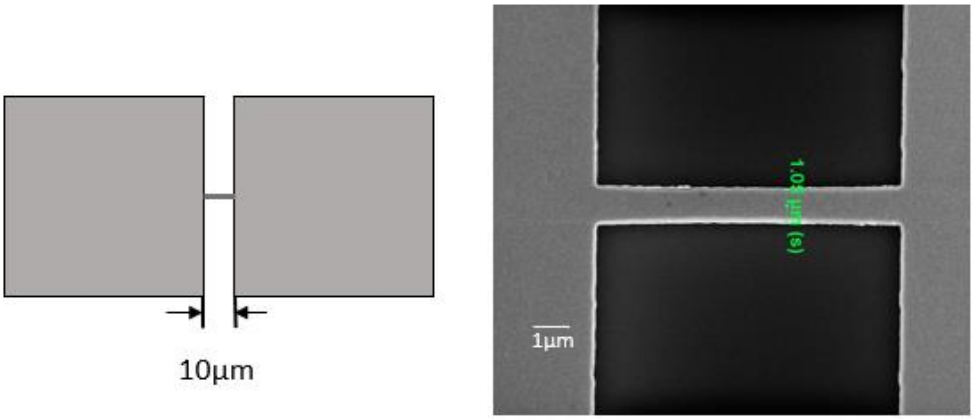


Figure 66. Dogbone Device for Measuring Resistivity.

positioned between two 120 μm square contact pads. The dogbones were fabricated on the same wafer coupon at the same time as the test devices. Kelvin probes were used to

drive a low (-1 mA to 1 mA) current. Wires with widths of 292 nm, 479 nm, and 1 µm were successfully fabricated and tested for the 100 nm thickness, while wires with lower dimensions and 50 nm thickness encountered difficulties with fabrication fidelity or wire failure during testing. Resistance measurements were obtain from the three dogbone configurations and resistivity values were calculated from the equation:

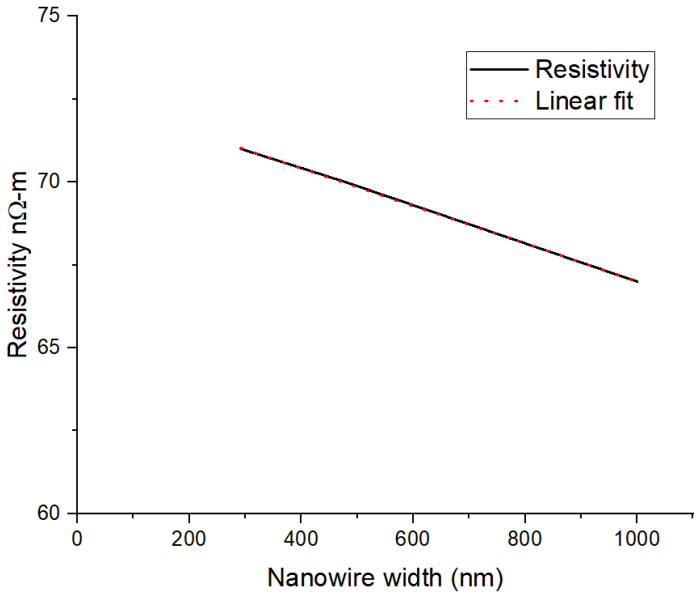


Figure 67. Dogbone Resistivity Testing, 100 nm Thickness at Room Temperature.

ρ=RA/L, where the dimensions for each dogbone were determined via high resolution SEM images. Figure 67 presents the results of the dogbone testing, which shows a slight decrease in resistivity with increasing wire width. Sheet resistivity measurements were also performed on a 100 nm thick Ti/Au film, using linear 4-point probe (Bridge Technology Jandel University probe with Keithley 2450 source meter). The four probes system is too large to land on the device itself, so measurements were performed on a Si witness coupon that was metallized concurrent to the devices. The four-point probe

measurement of 52.9 nΩ-m is significantly lower than the measured dogbone values. Disparities may be due to different substrate material (2μm thick SiO_2 on Si vs. Si wafer with native oxide), or poor ohmic contact of one or more of the probes. The 50 nm thick Ti/Au film was also measured using the linear 4-point probe, and a resistivity of 64.3 nΩ-m was recorded. These values are considerably greater than the bulk gold resistivity value of 24.2 nΩ-m.

Further attempts to produce and measure dogbone test structures at the nanoscale were not forthcoming. Therefore, another approach was developed to determine the resistivity of the nanowires used to determine thermal conductivity. At the nanoscale, the nanowires are expected to have a different resistivity than the RTDs and heaters due to mixed size regimes. Therefore, a simple resistance measurement is not sufficient for determining nanowire resistivity. This situation is exacerbated by the devices not being reducible to a combination of series and parallel resistors. The method developed here relies on FEA and a parametric sweep function in COMSOL® simulation to compare resistance measurements. As noted earlier in this chapter, the temperature response for each test device was measured and simulated so that the temperature of each nanowire array for a given drive current was determined. These data are found to be useful for estimating resistivity of the nanostructures studied, as presented next. The approach involves changing the terminal and ground of the device so the current is driven through sample RTD instead of the heater, as shown in the thermal response of Figure 68. Concurrent to the simulation shown in Figure 68, a parametric sweep was performed to determine the resultant nanowire array temperature over a range of resistivity values of the nanowire array. The parametric sweep is a stationary study and allows a specified

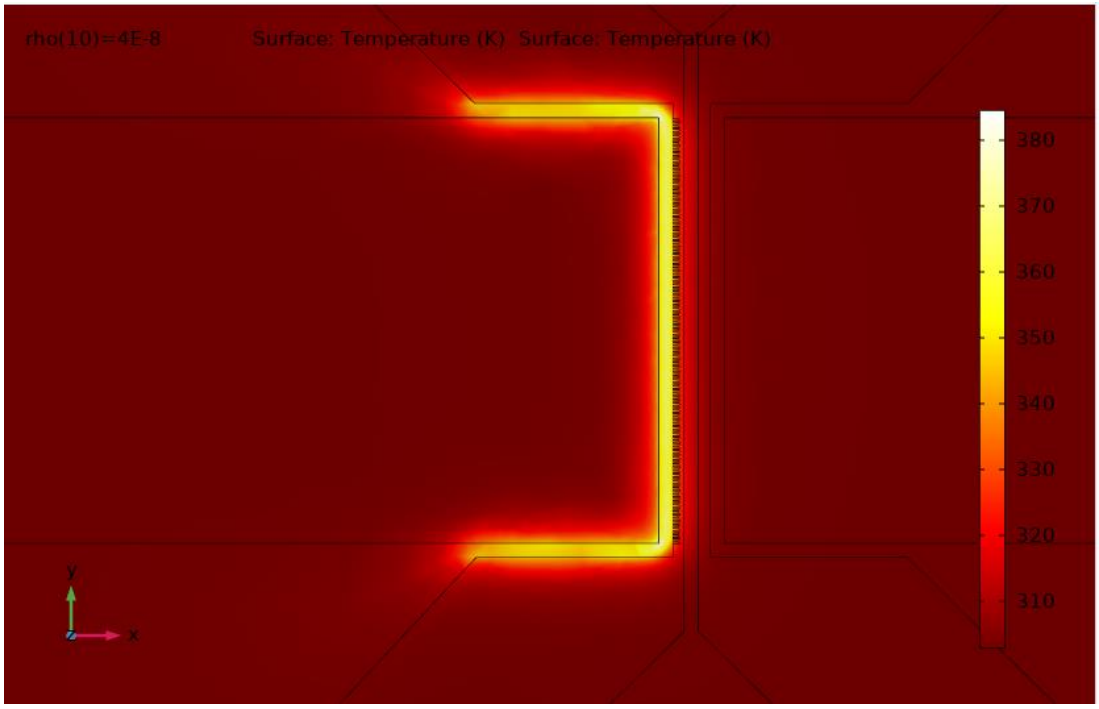


Figure 68. FEA Simulation of Drive Current Applied to Sample RTD

the range of parameter values to be evaluated during the simulation. Figure 69 presents the output of such a sweep, where the temperature of the nanowire array was estimated based on resistivity values of array ranging from 24 – 40 nΩ-m.

Next, the temperature response of the nanowire array for a given drive current from the previous simulations was recalled. For the device shown in Figure 68, the previous simulation indicated that the nanowire array reached an average temperature of 329.8K for a 25 mA drive current. The parameter sweep shown in Figure 69 indicates that in order to achieve a 329.8K average temperature, the nanowire resistivity must be approximately 34 nΩ-m. For this discussion, resistivities determined using this approach will be referred to as "Data/FEA." It is important to remember that the temperature used in this analysis has an uncertainty of ± 0.5K, which leads to an uncertainty of the nanowire resistivity of ± 0.1 nΩ-m.

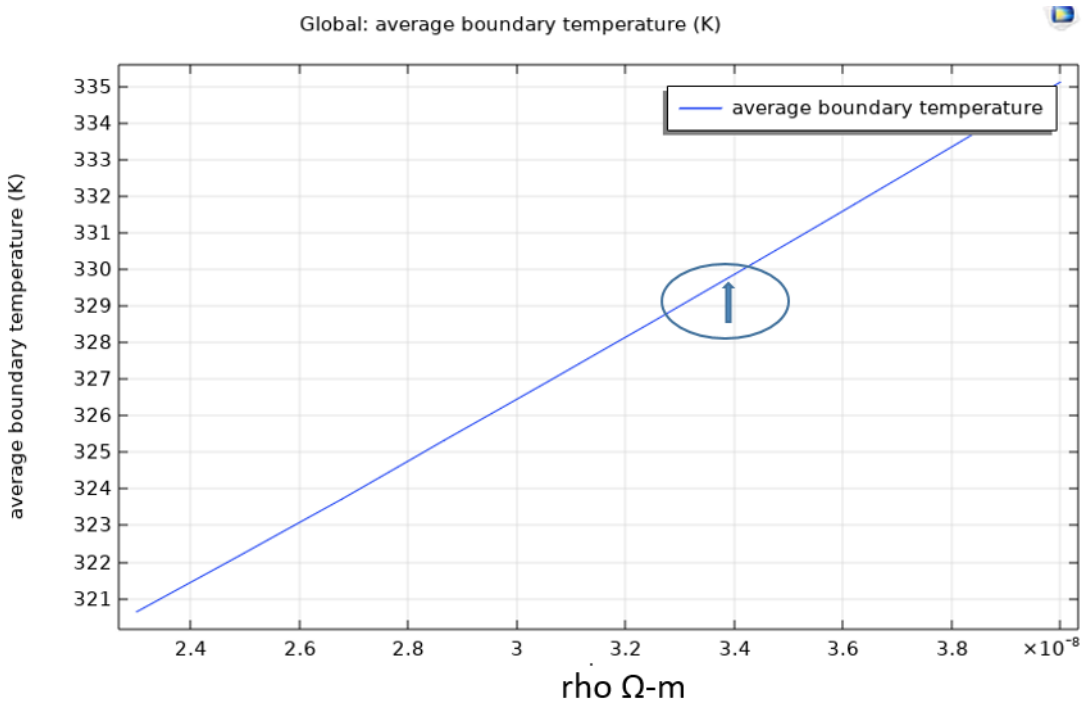


Figure 69. Parametric Sweep of Resistivity

The parametric sweep was performed on several different nanowire geometries for both the 50 nm and 100 nm thick devices to determine the resistivity, as shown in Figure 70, along with the dogbone measurements and the 4-point probe measurements. As expected, the resistivity values of the 100 nm thick devices (squares) were consistently lower than their 50 nm counterparts (triangles). Further, the dogbone measurement produced consistently higher resistivities than both the so-called Data/FEA measurements and the 4-point probe measurement for the 100 nm thickness level. Overall, the 100 nm thick samples appear to have little sensitivity to the nanowire width, over this range, producing generally flat results with increasing width.

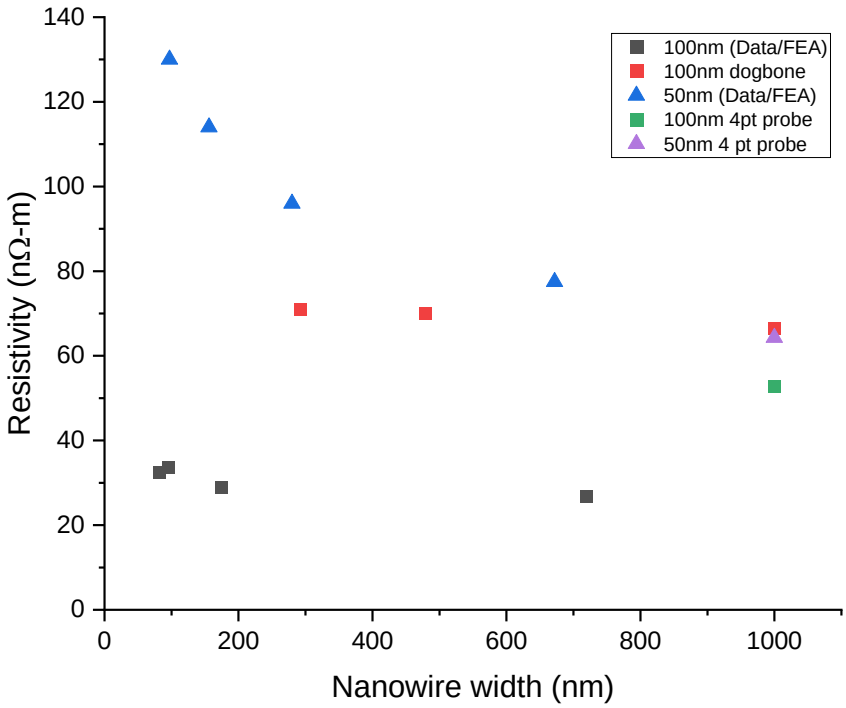


Figure 70. Experimental Resistivity Measurements at Room Temperature

However, the 50 nm Data/FEA resistivity measurements were shown to decrease with increasing nanowire width. Further, the 50 nm, 4-point probe tests appears to align with the trend of the 50 nm Data/FEA measurements. This data indicates that, for the 100 nm thickness level, the resistivity is relatively constant over a range of nanowire widths, while the resistivity of the 50 nm thickness level shows a strong dependence on nanowire width.

To further examine this behavior, the experimental resistivity (closed symbols) from this study was compared to literature values (open symbols) for the 100 nm conditions, as shown in Figure 71.

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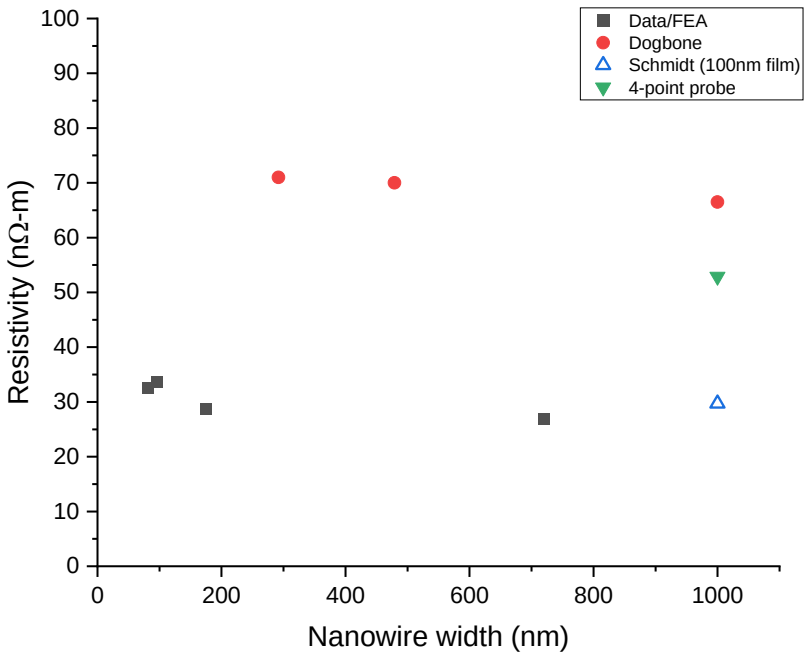

Figure 71. Comparison of 100 nm Thick Experimental Resistivity with Literature.

In the 100 nm data, the literature value from Schmidt *et al.* [66] is consistent with results from the Data/FEA approach. The Schmidt *et al.* data was derived from van der Pauw conductivity measurements using a Hall effect measurement system. Figure 72 presents the resistivity data for the lower (66nm and less) thickness wires and films, and shows a pronounced reduction with increasing nanowire width. The Data/FEA results are higher than literature values at the low dimensions, but good agreement is realized with increasing nanowire width.

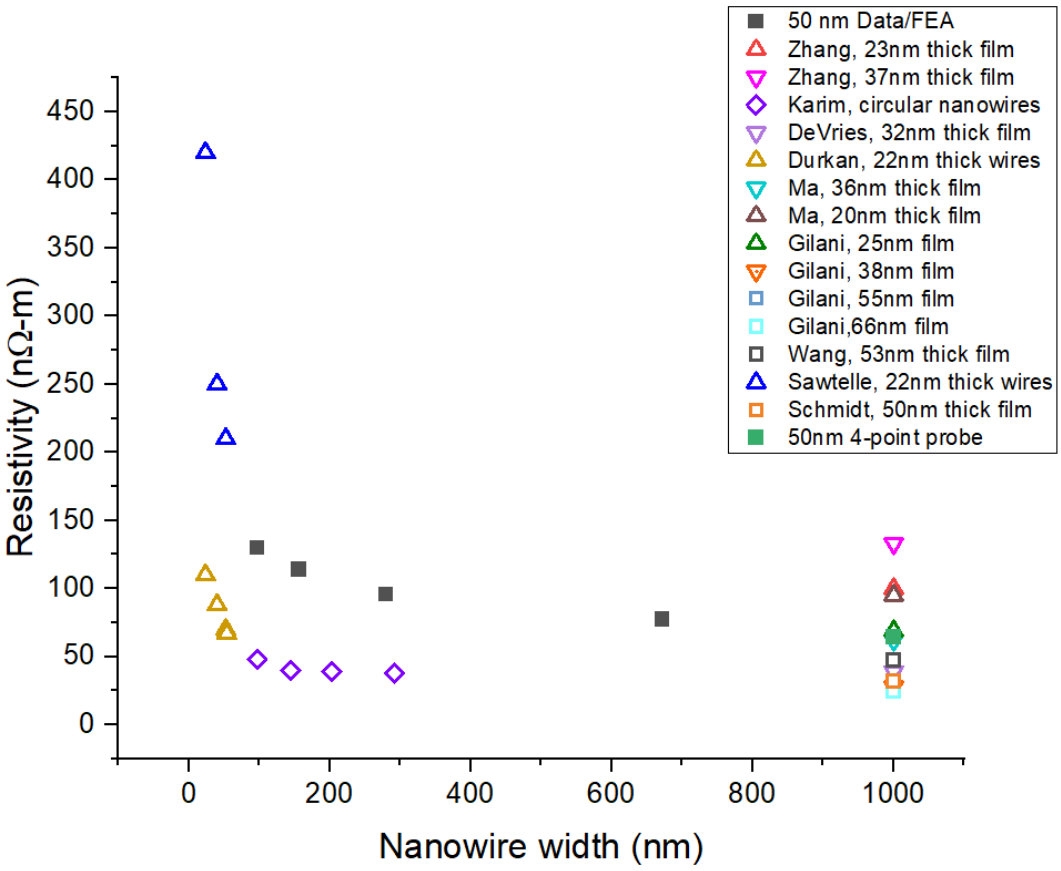

Figure 72. Resistivity vs. Nanowire Width, Experimental (50 nm thick) with Literature. (dimensions noted)

There is a dependence of resistivity with nanowire dimension for the 50 nm thick devices that is not observed with the 100 nm conditions. This dependency is particularly apparent in the work of Sawtelle, Karim, and Durkan with low dimension nanowires. This suggests that “structural scattering” of surfaces and interfaces, in addition to grain boundaries and impurities, are playing a prominent role in the scattering of electrons, thus increasing the electrical resistivity.[4]

6.5 Wiedemann-Franz Law

As discussed previously in Chapter 2, the Wiedemann-Franz (W-F) law is an approximation that relates thermal conductivity to electrical conductivity at a specified temperature. While considered robust for many bulk materials, the W-F law is often violated at the nanoscale, in part due to the absence of phonon transport contributions and inelastic scattering, particularly in polycrystalline structures. [109, 126]

Recall from Equation (8) W-F law is expressed as

$$\kappa = \sigma L T \tag{8}$$

where κ is the thermal conductivity, σ is the electrical conductivity, and T is the absolute temperature in Kelvin. This equation can be solved for κ for the test devices using the empirical resistivity (1/σ) data generated in this study for a specific temperature and the Lorenz number. As shown in Table 2, the Lorenz number is temperature-dependent and varies significantly for different metals.

In the research of Sawtelle *et al.*, values of the Lorenz number were calculated for gold nanowires over a wide range of temperatures using several different estimation methods, as shown in Figure 73. These estimation methods attempt to include the influence of the substrate on the resultant L value. The comparisons are made for nanowires supported on a SiO_2 substrate (variable $k_{ox}(T)$) and constant k_{ox} (298K), and nanowires that a suspended ($k_{ox} = 0$) The suspended nanowire data was acquired from the work of Cheng *et al.* and Volklein *et al.*[65, 127] The variable $k_{ox}(T)$ condition, denoted by the filled circle, is intended to account for substrate heat sinking in the model,

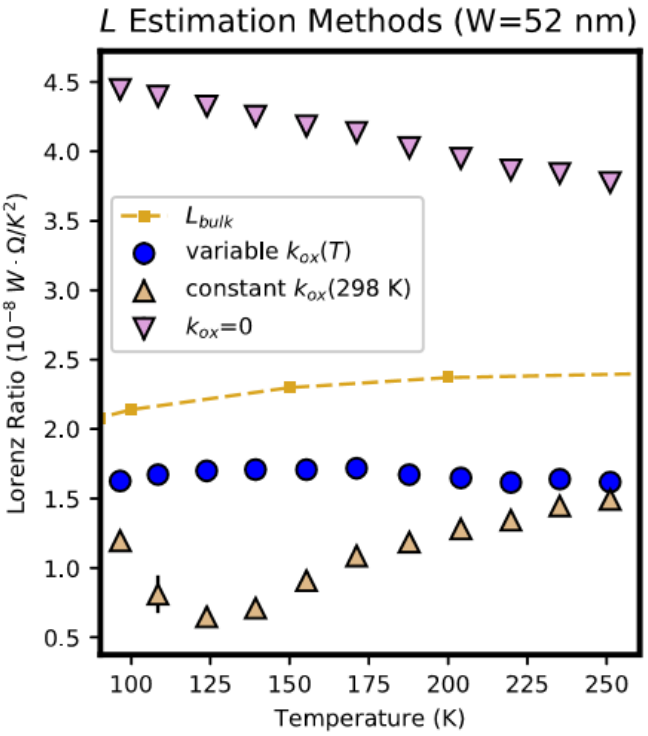

Figure 73. Comparison of Lorenz Number Values of Gold Nanowires. (22 nm thick, 52 nm wide) using three different estimation methods [4]

and is considered to be the most "physically" correct of the three methods evaluated. The bulk value of L is also included for comparison.

The estimated L values at 250K shown in Figure 73, along with the theoretical L_{bulk} value, were used in Equation (8) to calculate thermal conductivity using the empirical resistivity values from the present study. The calculated thermal conductivity values are compared to the corresponding experimental values, as shown in Figure 74. The three curves represent the calculated values of thermal conductivity using the W-F law and the measured resistivity values at 298K for 50 nm thick nanowires ranging in width from 97 nm to 642 nm. The green filled circles represent the experimental thermal conductivity results for the corresponding 50 nm thick nanowires. The experimental

thermal conductivity value for the 22 nm thick, 50 nm wide condition from Sawtelle *et al.* is also shown.

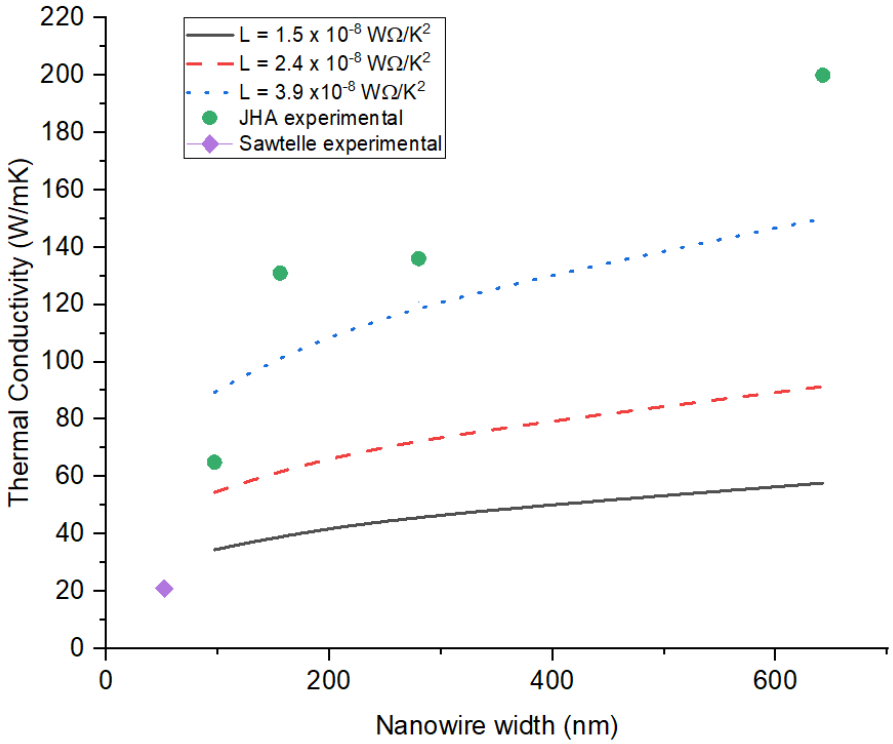

Figure 74. Effect of the Lorenz Number Estimates on Thermal Conductivity. (with 50 nm experimental data included)

At 97 nm width, the experimental thermal conductivity data coincides best with the calculated value the L_{bulk}. Increased widths deviated significantly from the predicted values using the three different L values. The data further suggests that, in order for the W-F law to fit the experimental data, the L values would have to be significantly higher than the proposed models in the Sawtelle study. This is consistent with the findings of many researchers, who theorized that elevated L values are warranted in the W-F law to account for the aforementioned phonon scattering and inelastic scattering that occurs at the nanoscale. [24, 109, 127-129]. Burkle *et al.* observed that L can increase as much as

30% in gold nanostructures as compared to bulk [126], while Wang *et al.* found L values of nanostructures were 1.3 to 1.8 times larger than bulk.[130]

It is important to highlight the many differences present when applying the models from Sawtelle to the current study. First, the Sawtelle models were generated from wires that were more than half the thickness of the present study.

Secondly, the thickness of the SiO_2 substrate used in the Sawtelle study was very thin (22 nm thick) as compared to the 2 μm thick $Si0_2$ layer substrate in the present study. As demonstrated in the simulation work presented in section 4.2, considerable heat dissipation occurs into the substrate with thin oxide layers. The impact of this heat dissipation, or heat sinking, affects not only thermal conductivity but the coupled response of electrical resistivity. The Sawtelle study attempts to correct for this heat-sinking with the variable $k_{ox}(T)$, which results in an L value that is actually less than bulk. Further, the Sawtelle samples did not use an adhesion layer when fabricating the gold nanowires, leading to highly granular structure which may support additional "Lamb-type" vibrations that impact inelastic scattering. Depressed L values on the nanoscale were also found in studies involving silver nanowires. [65, 131]

The Wiedemann-Franz law does not adequately predict the thermal behavior the gold nanostructures in this study. This is not surprising, as many researchers have demonstrated violations of the law. Attempts to adjust the Lorenz number to account for the specific conditions of nanoscale thermal transport were not readily applicable to this study. The observed violation of the Wiedemann-Franz law suggests that scaling of gold nanowires has a relatively different impact on electrical conductivity and thermal conductivity. In other words, the extent of the reduction in electrical conductivity

observed in gold nanowires is different than the reduction in thermal conductivity. Thermal conductivity and electrical conductivity may exhibit differences in sensitivity to specular boundary conditions and grain boundary scattering that contribute to Wiedemann-Franz law violations.

6.6 Electron and Phonon Contributions to Thermal Conductivity

Violations of the Wiedemann-Franz law are often attributed to neglecting the phonon contribution to thermal conductivity at the nanoscale. Stojanovic *et al.* developed a method of modeling this contribution κ_{ph} by solving the Boltzmann Transport Equation (BTE) and applying boundary conditions of partially specular scattering developed by Fuchs.[47, 62]

Table 10. Bulk Thermal Conductivities and Phonon Contributions[47]

Metal	κ(bulk)	κ(ph) BTE	κ(ph) MD
Au	317	5	4.1
Ag	429	9.3	7.7
Cu	401	22.2	18
Al	237	21.1	21
Ni	90.7	9.6	15.8
Pt	71.6	8.3	11.7
W	170	42.2	--

Table 10 presents two methods of calculating the phonon contribution of thermal conductivity for commonly used electronic materials using BTE and molecular dynamics (MD) models. Included in the table are the corresponding bulk values. For gold, the κ_{ph} was determined to by 5 W/mK using BTE, which is consistent with κ_{ph} = 4.1 using calculations from the MD model.[132] This is a very small contribution to the overall

thermal conductivity, suggesting that gold thermal transport is largely electronic in nature κ_e, as compared to κ_{ph} = 21.1 W/mK for aluminum and κ_{ph} = 22.2 W/mK for copper.

Scaling also plays a significant role on both κ_{ph} and κ_e. Stojanovic et al. calculated the thermal conductivities of square cross-section nanowires of various metals using the BTE model, and compared the effect of scaling on the electron and phonon constituents. Figure 75 presents the calculated electronic thermal conductivity κ_e for gold nanowires with square cross-sections as well as the experimental data from the current study (JHA data) and literature data.[4, 47, 61, 120]

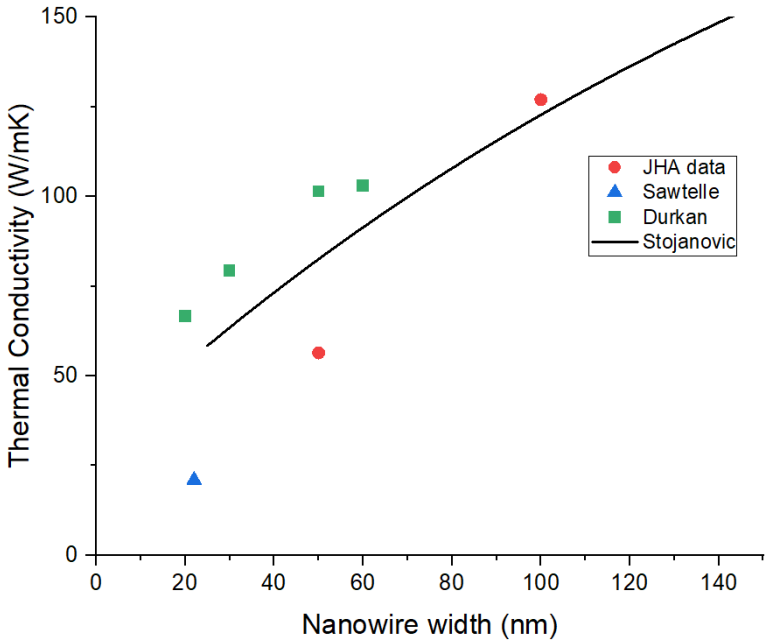

Figure 75. Comparison of BTE-determined Thermal Conductivity.
with Experimental and Literature Values

The two JHA data points reflect dimensions close to a square cross-section. Generally good agreement is seen between the model and experimental results,

confirming that the phonon contribution to the overall thermal conductivity in gold nanowires is minimal. Further, the model is shown to be valid for gold nanowires and is predictive of the dimensional response.

It is apparent that direct measurements are necessary for understanding the properties of nanoscale materials, and estimations based solely on electrical properties fail to adequately predict their thermal response. This was previously demonstrated by Stojanovic, *et al.,* for aluminum nanowires. [49] The work reported here, on gold nanofilms and nanowires, further supports the validity of the theoretical work presented by that same group.[133] It should be noted that the experimental validation is supported down to the 20-40 nm length scale.

7. CONCLUSIONS AND FUTURE WORK

The trend towards scaling continues in microelectronic devices and a vast array of new, emerging fields spanning multiple scientific disciplines. [1, 39-46] This scaling poses significant challenges to designers and manufacturers alike, highlighting the importance of understanding material properties and their relative impact on thermal behavior. Gold has consistently played a central role in these technologies motivating studies of its properties at the nanoscale.

In this dissertation, a direct measurement technique, initially proposed and developed by Stojanovic *et al.*, was further extended and used to measure the thermal conductivity of gold nanostructures ranging in dimension from 74 nm to 720 nm in width at two thickness levels, 50 nm and 100 nm. Key modifications were introduced into this testing method and analysis, as listed below.

- E-beam lithography was central to patterning. Here it was used in fabrication of both the test device and the subject nanostructures rather than a combination of photo- and e-beam-lithographies. Solely utilizing e-beam lithography has the advantage of eliminating alignment issues between patterning steps since all patterning is done in a single SEM writing session for the simultaneous fabrication of the heater, sensors, and the nanostructures themselves
- Electrical testing was performed using a quasi-steady state I-V sweep, as opposed to a steady-state drive current. Implementation of this automated protocol allowed for 98 repeat measurements for each sweep. Use of the I-V sweep also allowed for characterization of the material during joule heating to device failure.

- A parameter estimation optimization algorithm incorporating the I-V sweep measurements into the FEA simulations to determine the thermal conductivity of each nanowire geometry.
- Testing results were obtained for both room temperature and 100°C to explore the thermal response of gold nanostructures under simulated operating conditions within a device.

7.1 Contributions of This Work

The findings in this dissertation contribute empirical data to the body of knowledge regarding the thermal behavior of nanostructured gold, and can be used to validate or disprove theoretical predictions in literature. A main objective of this research was to utilize an existing test method for measuring thermal conductivity and expand its functionality and analysis capabilities to further explore the impact of size effects on nanostructured gold.

First, the ability to measure and discern differences in thermal conductivity of gold with varying dimensions was demonstrated. This work spans a wide range of dimensions for 74 nm width nanowires to nanofilms. The ability to generate these different dimensions on the same wafer under the same processing conditions eliminates much of the inherent variability and complexity of fabrication. The central contribution to this research area is presented in Figure 54 that shows the effect of nanoscale dimension on thermal conductivity for gold. Available data from the literature are also included. The overall trend observed is supported by all available data.

Second, the effect of temperature on thermal conductivity of the gold nanostructures was explored and again, the testing methodology was capable of

determining differences among different dimension scales. Results of these investigations are shown in Figures 59-65.

Based on these studies, the method was found to be robust for measuring thermal conductivity. Deviations from the ideal nanofabrication still resulted in thermal conductivity values that fell within the data range.

Finally, the empirical data were used to test the validity of several theoretical models.[4, 61, 133] Possible deviations from the predictive models were suggested. Further, trends in the empirical data point to a length scale parameter, independent of deposition thickness or testing temperature, which likely, in part, dictates thermal behavior.

This research will be submitted for peer-review publication.

7.2 Suggestions for Future Work

Further investigation of nanoscale thermal properties using the microelectrothermal testing device, along with the electrical testing protocols and FEA simulation work, is warranted. Future testing should be expanded to include additional materials, particularly those materials identified as potential replacement candidates for copper interconnects, such as cobalt and ruthenium. These alternate materials have very low MFP values, as shown in Table 1, making them less sensitive to size effects. [134]

The overall effect of grain size and morphology on thermal properties should also be studied. Post-processing heat treatments and different metallization methods would provide much needed understanding to the role of structural scattering on thermal and electrical transport and how to optimize microstructure. Also, post-processing heat treatments could provide the opportunity to “decouple” deposition thickness with grain

size.

Further investigation of the effect of temperature on thermal conductivity should also be explored. Both elevated temperature testing as well as low temperature testing would provide additional insights into scattering mechanisms and predictive modeling for in-service applications.

Fabrication and testing of "dogbone" structures for resistivity measurement should be revisited. Difficulties in generating uniform wires between the contact pads needs to be addressed.

An investigation of the role of roughness on understanding the nature of electron scattering (specular vs. diffuse) should be considered. Modifications to roughness could be achieved by use of different adhesion layers, such as self-assembled monolayers, or by post-processing treatments like argon cleaning. Such roughness changes could be characterized via atomic force microscopy. Further, AFM characterization would be helpful to confirm flatness and sidewall integrity following the lift-off process.

Determination of the maximum aspect ratio for this fabrication process would be helpful to further explore a larger thickness range. By expanding the thickness range, it would be interesting to determine at what point the measured thermal conductivity values agrees with bulk values.

Although direct writing of nanowires proved unsuccessful in the case of cobalt, the use of FEBID for nanowire generation should be revisited. Perhaps platinum, frequently found on SEM GIS systems, could be used to generate nanowire and nanofilms for thermal conductivity testing and compared to existing literature data.

Finally, similar to industry trends, this study should be advanced to even lower

dimensions than 74 nm. Based on the pitch study and the relative insensitivity to fill factor, low width nanowires may be fabricated without requiring a high density of the wires within the array, resulting in a greater likelihood of patterning and lift-off success during fabrication.

APPENDIX SECTION

This section provides detailed information of the FEBID efforts to produce cobalt nanowires, as described in Section 4.6.

A canister of dicolbalt octacarbonlyl ($Co_2(CO)_8$) was installed on the SEM as the precursor gas for deposition and a fine needle is inserted into the chamber to introduce the gas directly above the sample. A bitmap of the desired pattern was uploaded into the SEM GIS control software to direct the beam. The electron beam is used to decompose the gas into volatile and non-volatile components. The volatile components of the gas are removed by the SEM vacuum system, while the non-volatile components are deposited

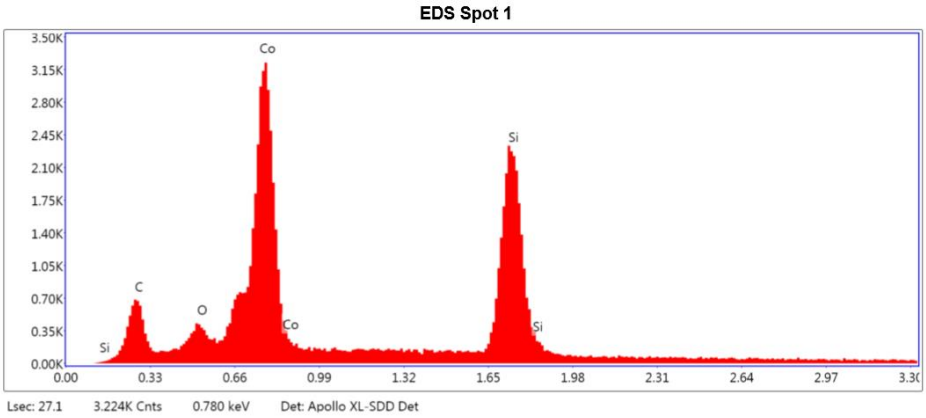

Figure 76. EDS Spectrum of FEBID Cobalt Nanowires

on the sample in the desired pattern. Beam current and dwell times dictate the deposition thickness of the material. Prior to deposition, the precursor gas is heated to 27°C.

One of the main concerns of FEBID is the purity of the deposited material, which can be impacted by several factors including beam current and potential beam-induced heating. Studies suggest that the atomic weight percentage of cobalt in FEBID depositions ranges between 80-90%.[135-137] In the present study, the cobalt nanowires generated from

FEBID had an approximate atomic weight percent range of 72 - 93%, as determined by energy dispersive x-ray spectroscopy (EDS), as shown in Figure 76. The silicon on the spectrum represents the wafer coupon that the nanowires were deposited on, while the carbon and oxygen are impurities found in the deposition likely originating from incomplete dissociation of the precursor molecules and the environment within the SEM chamber.[138] The age of the precursor gas is also believed to impact the purity of the deposited material. Purification methods, either *in situ* or *ex situ*, have been investigated by other researchers, including extensive procedures to clean and de-gas the SEM chamber and components.

Cobalt nanowires using the technique described above are shown in Figure 77. The nanowire array was positioned between the sample RTD and heater, with each individual nanowire width measuring 33nm. The width and deposition thickness of the nanowires appear uniform, with no apparent irregularities along the length of the wires.

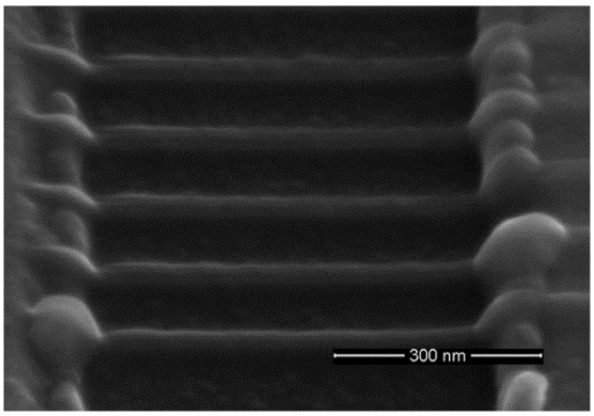

Figure 77. Cobalt Nanowire "Ladder" at 45° Tilt

Significant build-up is evident at the interfaces between individual nanowires and the gold RTD and heater traces. Adjustments to the bitmap could presumably remedy this situation. Unfortunately, a large obstacle to this technique is the over-spray of the cobalt

material to areas in the vicinity of the nanowires. Figure 78 illustrates the effect of the overspray by an EDS map.

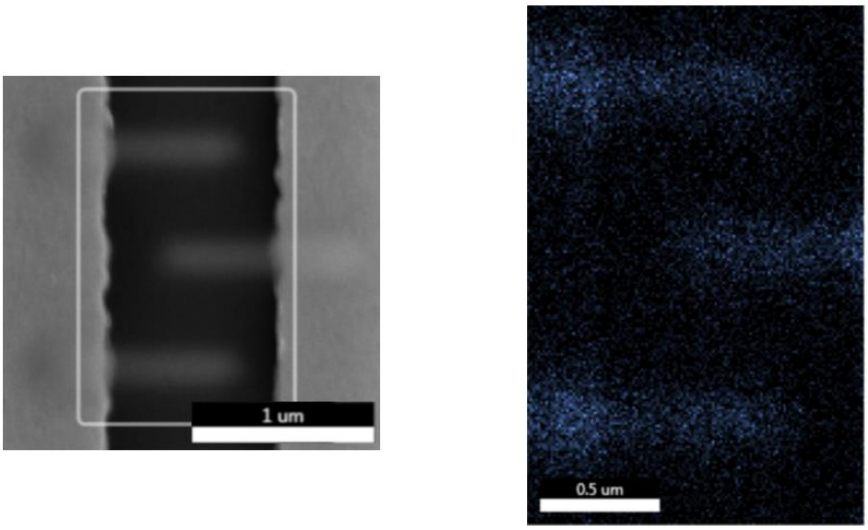

Figure 78. EDS Mapping of Cobalt Nanowires

The image on the left is a set of interdigitated cobalt nanowires generated by the FEBID process on a test structure. The wires are located between the sample RTD and the heater trace. Distortion of the photo can be attributed to the relatively high beam currents necessary to achieve a high x-ray count for the EDS system. Also, the ferromagnetic nature of the cobalt wires proved to contribute to the difficulty in imaging the samples. The image on the right is the EDS mapping of cobalt (in blue) of the boxed area shown in the photo on the left. As expected, high levels of cobalt are concentrated in the interdigitated wires, but a significant over-spray of cobalt is also evident between the wires. The overspray, also known as “halo” or “proximity” effects, is well-documented in literature [135, 139, 140] Nikulina et al. states that mainly secondary electrons (SE) are responsible for the precursor dissociation necessary for deposition. The secondary electrons take two forms: SE_I which are responsible for the deposition of the material at

the surface, and SE_{II} which are created by energetic back-scattered electrons (BSE). It is the SE_{II} component that contributes to the formation of an overspray around the main deposit, thus reducing lateral resolution. For some applications, the presence of an overspray has negligible impact on the intended functionality of the deposited material.

In this study, however, the presence of this overspray was found to adversely affect the electrical testing of the test structures, resulting in electrical shorts between RTDs. Attempts were made to eliminate or minimize the presence of the overspray through post-processing treatments that would not adversely affect the morphology of the deposited wires. Argon cleaning and O_2 ash processes were evaluated, but had minimal impact on overspray removal. More aggressive techniques, such as ion milling were also tested, but resulted in damaging the wires and unintended embedding of Ga^+ in the substrate from the ion beam source.

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